CC4500AC55FB Conduction Cooled Wide-Output-Range Power Supply

Input: 185-300V_{AC} ; 4500W Capable; Outputs: 40-58V_{DC}, 5V_{DC}@10W

The CC4500AC55FB has a wide programmable output voltage capability. Featuring high-density, fully enclosed, conduction-cooled packaging, it is designed for minimal space utilization and is highly expandable for future growth. This CC4500 incorporates both RS485 and dual-redundant I^2C communications busses that allow it to be used in a broad range of applications. Feature-set flexibility makes this CC4500 an excellent choice for applications requiring operation over a wide output-voltage range.

Applications

- Supercomputers
- Telecom central offices
- Industrial systems
- RF Energy systems
- Wide band power amplifier
- Broadcast systems
- Lasers

Features

- Efficiency exceeding 96 % - 80+ Titanium rating
- Compact 1RU form factor with 41.8 W/in^3 density
- 4500W from 185-300V_{AC} up to 60°C case
- Output voltage programmable from 40V_{DC} – 58V_{DC}
- ON/OFF control of the main output
- Comprehensive input, output and over-temperature protections
- PMBus compliant dual I^2C serial bus and RS485
- Remote firmware upgrade capable
- Power factor correction (meets EN/IEC 61000-3-2 requirements)
- Redundant, parallel operation with active load sharing
- Redundant +5V @ 2A Aux power
- Completely enclosed, conduction cooled
- Hot insertion/removal (hot plug)
- Four front panel LED indicators
- UL* Recognized, CAN/ CSA† C22.2 specified compliance with IEC62368-1
- CE mark meets 2014/35/EU directive
- RoHS Directive 2011/65/EU and amended Directive (EU) 2015/863

* UL is a registered trademark of Underwriters Laboratories, Inc.

† CSA is a registered trademark of Canadian Standards Association.

§ This product is intended for integration into end-user equipment. All CE marking procedures of end-user equipment should be followed. (The CE mark is placed on selected products.)

** ISO is a registered trademark of the International Organization of Standards

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

Parameter	Device	Min	Max	Unit
Input Voltage: Continuous	V_{IN}	0	300	V_{AC}
Operating Case Temperature (sink side)[1]	T_C	-20	75[2]	°C
Storage Temperature	T_{stg}	-40	85	°C

Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, Vo = $55V_{DC}$, resistive load, and temperature conditions.

INPUT

Parameter	Symbol	Min	Typ	Max	Unit
Startup Voltage High-line Operation	V_{IN}			170	V_{AC}
Operating Voltage Range High-line Configuration		170	200 - 277	300	
Voltage Swell (no damage)		320			
Turn OFF Voltage Hysteresis		140 10	150	160	
Frequency	F_{IN}	47		66	Hz
Source Impedance (NEC allows 2.5% of source voltage drop			0.2		Ω
Operating Current; at $230V_{AC}$ at $277V_{AC}$	I_{IN}		 20.49 16.92		A_{AC}
Inrush Transient ($277V_{RMS}$, 25°C, excluding X-Capacitor	I_{IN}		25	45	A_{PK}
Idle Power (at $277V_{AC}$, 25°C) 55V OFF 55V ON @ Io=0	P_{IN}		 12 15		W
Leakage Current ($277V_{AC}$, 60Hz)	I_{IN}		2.5	3.5	mA
Power Factor (20% load for Min – 50-100% load for Typ)	PF	0.95	0.995		
Efficiency[3], $230V_{AC}$, $55V_{DC}$, @ 25°C 10% of FL 20% of FL 50% of FL 100% of FL	η	 91 94 96 94			%
Holdup time 55V/4500W, output allowed to decay down to $40V_{DC}$ For loads below 1500W	T	10 15			ms
Ride through (at $230V_{AC}$, 25°C, 50Hz)	T	1/2	1		cycle
Power Good Warning[4] (main output allowed to decay to $40V_{DC}$)	PG	3	5		ms

[1]See the derating guidelines under the Environmental Specifications section

[2]From 50°C-75°C see derating guidelines

[3]5V output at 0A load.

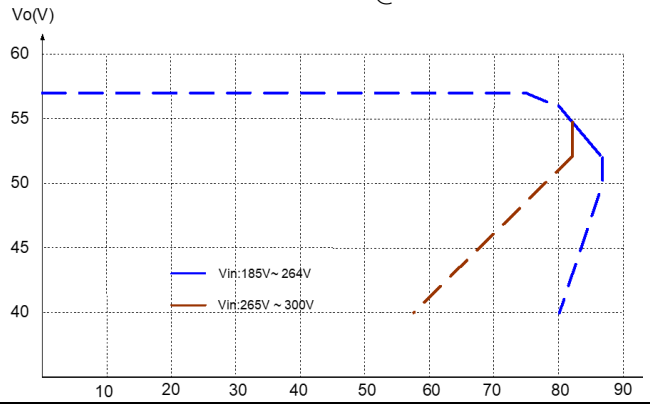
[4]Internal protection circuits may override the PG signal and may trigger an immediate shutdown. PG should not indicate normal (HI) until the main output is within regulation. PG should be asserted if the main output is about to shut down for any detectible reason.

Electrical Specifications (continued)

55V_{DC} MAIN OUTPUT

Parameter	Symbol	Min	Typ	Max	Unit
Output Power[5] @ 170V_{AC}, TC < 50°C @ High line input 200 – 277V_{AC}[6], V_O > 44V_{DC}, T_C < 50°C	W	3600 4500			W_{DC}
Factory set default set point	V_{OUT}		55		V_{DC}
Overall regulation (load, temperature, aging) 0 - 45°C LOAD > 2.5A > 45°C		-1 -2		+1 +2	%
Output Voltage Set Range		40		58[(9)]	V_{DC}
Response to a ΔV ≤ 10V Vprog change command Response to a ΔV ≤ 10V i²C instruction	T			200 50	ms
Output Current @ 4500W (200 – 277V_{AC}), 55V	I_{Out}	1		82	A_{DC}
Current Share > 20% FL V_O > 42V_{DC} V_O < 42V_{DC}		-5 -10		5 10	%FL
This CC4500 must be able to operate within all of its rated specifications with 2 to 36 connected in parallel.					
Output Ripple (20MHz bandwidth, load > 1A) RMS (5Hz to 20MHz) Peak-to-Peak (5Hz to 20MHz)	V_{OUT}			100 500	mV_{rms} mV_{p-p}
External Bulk Load Capacitance	C_{OUT}	0		56,000	mF
Turn-On (monotonic Turn-ON from 30 – 100% of Vnom above 5°C) Delay Rise Time – PMBus mode Rise Time – RS-485 mode[7]	T		4 120 10		s ms s
Output Overshoot	V_{OUT}			2	%
Permissible Load Boundary – Power Limit	P_{OUT}	4500			W

The overload current limit threshold should be set @ 2% above the load envelope shown here



Vin: 185V ~ 264V								
Vo (V)	40	42	48	52	53	55	56	58
Io (A)	80	81	85	86.5	85	82	80.3	75.5

Vin: 265V ~ 300V								
Vo (V)	40	42	48	52	53	55	56	58
Io (A)	58	63	74	78	85	82	80.3	75.5

[5]Output power capability is proportional to output voltage setting, see the permissible load boundary

[6]Input line range: 200 – 277 V_{RMS} (±8%)

[7]Below -5°C, the rise time is approximately 5 minutes to protect the bulk capacitors.

Electrical Specifications (continued)

$55V_{DC}$ MAIN OUTPUT (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Overvoltage - 200ms delayed shutdown Immediate shutdown	V_{OUT}	> 60		< 65	V_{DC}
Latched shutdown	Three restart attempts are implemented within a 1 minute window prior to a latched shutdown.				
Over-temperature warning (prior to commencement of shutdown Shutdown (below the max device rating being protected) Restart attempt Hysteresis (below shutdown level)	T		5 20 10		°C
Isolation Output to Chassis	V	500			V_{DC}

$5V_{DC}$ Auxiliary Output (return is Logic_GND)

Parameter	Symbol	Min	Typ	Max	Units
Output Voltage Setpoint	V_{OUT}		5		V_{DC}
Overall Regulation		-3		+3	%
Output Current		0.005		2	A
Ripple and Noise (20mHz bandwith)			50	100	mV_{P-P}
Over-voltage Clamp				7	V_{DC}
Over-current Limit		110		175	%FL
Isolation Logic_GND to Chassis		100			V_{DC}

Hold up time stand-by rail. The stand-by rail must remain within regulation for 2s following loss of AC, at full load (10W).

The $5V_{DC}$ should be ON before availability of the $55V_{DC}$ main output and should turn OFF only if insufficient input voltage exists to provide reliable $5V_{DC}$ power. The PG# signal should have indicated a warning that power would get turned OFF and the $55V_{DC}$ main output should be OFF before interruption of the $5V_{DC}$ output. But, it should not be the case during Firmware Upgrade with CC4500AC55FB version.

General Specifications

Parameter	Min	Typ	Max	Units	Notes
Reliability		1,000,000		Hours	Full load, 25°C ; - MTBF per SR232 Reliability protection for electronic equipment, issue 2, method I, case III,
Service Life		10		Years	At 80% load & 40°C cold plate
Unpacked Weight		2.8		kgs	
Packed Weight		3.3		kgs	
Heat Dissipation	200 Watts @ 80% load, 270 Watts @ 100% load				

Signal Specifications

Unless otherwise indicated, specifications apply overall operating input voltage, resistive load, and temperature conditions. Signals are referenced to (Logic_GND) unless noted otherwise. Fault, PG#, OTW, and Alert need to be pulled HI through external pull-up resistors.

Parameter	Symbol	Min	Typ	Max	Unit
ON/OFF Main output OFF 55V output ON (should be connected to Logic_GND)	V_{OUT} V_{OUT}	$0.7V_{DD}$ 0	— —	5 0.5	V_{DC} V_{DC}
Margining (by adjusting Vprog; see "Voltage programming" section) Programmed output voltage range Linear voltage control range Voltage adjustment resolution (8-bit A/D) Output set to $55V_{DC}$ Output set to $40V_{DC}$ $58 – 40V_{DC}$, settling time to new value	 V_{OUT} $V_{control}$ $V_{control}$ $V_{control}$ $V_{control}$ T	 40 > 0.1 3.0 0 —	 3.3 TBD	 58 < 3.0 3. 3 0.1 TBD	 V_{DC} V_{DC} mV_{DC} V_{DC} V_{DC} ms
Interlock	[short pin shorted to VOUT- on system side]				
Module Present	[short pin to Logic_GND internally]				

Signal Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Over Temperature Warning (OTW#) Logic HI (temperature normal)	V	$0.7V_{DD}$	—	12	V_{DC}
Sink current [note: open collector output FET]	I	—	—	5	mA
Logic LO (temperature is too high)	V	0	—	0.4	V_{DC}
Power Good (PG) Logic HI (temperature normal)	V	$0.7V_{DD}$	—	12	V_{DC}
Sink current [note: open collector output FET]	I	—	—	5	mA
Logic LO (temperature is too high)	V	0	—	0.4	V_{DC}
Protocol select Logic HI - Analog/PMBus™ mode	V_{IH}	2.7	—	3.5	V_{DC}
Logic – intermediate – RS485 mode	V_{II}	1.0		2.65	V_{DC}
Logic LO – DSP reprogram mode	V_{IL}	0	—	0.4	V_{DC}
Fault# Logic HI (No fault is present)	V	$0.7V_{DD}$	—	12	V_{DC}
Sink current	I	—	—	5	mA
Logic LO (Fault is present)	V	0	—	0.4	V_{DC}
Alert# (Alert#_0, Alert#_1) Logic HI (No Alert - normal)	V	$0.7V_{DD}$	—	12	V_{DC}
Sink current [note: open collector output FET]	I	—	—	5	mA
Logic LO (Alert# is set)	V	0	—	0.4	V_{DC}
SCL, SDA (SCL_0/1, SDA_0/1) Logic HI	V	2.1	—	12	V_{DC}
Sink current [note: open collector output FET]	I	—	—	5	mA
Logic LO (Alert# is set)	V	0	—	0.4	V_{DC}

Digital Interface Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
PMBus Signal Interface Characteristics[8]						
Input Logic High Voltage (CLK, DATA)		V	2.1		12	V_{DC}
Input Logic Low Voltage (CLK, DATA)		V	0		0.8	V_{DC}
Input high sourced current (CLK, DATA)		I	0		10	µA
Output Low sink Voltage (CLK, DATA, ALERT#)	I_{OUT}=3.5mA	V			0.4	V_{DC}
Output Low sink current (CLK, DATA, ALERT#)		I	3.5			mA
Output High open drain leakage current (CLK, DATA, ALERT#)	V_{OUT}=3.6V	I	0		10	µA
PMBus Operating frequency range	Slave Mode	FPMB	10		400	kHz
Measurement System Characteristics						
Clock stretching		$T_{stretch}$			25	ms
I_{OUT} measurement range		I_{rng}	0		100	A_{DC}
I_{OUT} measurement accuracy 25°C	> 16.5A < 16.5A	$I_{out(acc)}$	-1 5		+1 5	% of FL %
I_{OUT} measurement accuracy 0 – 40°C[9]	> 16.5A	$I_{out(acc)}$	-2		+2	% of FL
V_{OUT} measurement range		$V_{out(rng)}$	0		70	V_{DC}
V_{OUT} measurement accuracy[10]		$V_{out(acc)}$	-1		+1	%
Temp measurement range		$Temp_{(rng)}$	0		150	°C
Temp measurement accuracy[11]		$Temp_{(acc)}$	-4		+4	°C
V_{IN} measurement range		$V_{in(rng)}$	0		320	V_{AC}
V_{IN} measurement accuracy @ 25°C	V_{IN} > 120V_{AC} V_{IN} < 120V_{AC}	$V_{IN(acc)}$	-1.25 -2		+1.25 +2	%
I_{IN} measurement range		$I_{IN(rng)}$	0		30	I_{AC}
I_{IN} measurement accuracy – standard measurement @ 25°C		$I_{IN(acc)}$	-4		+4	% of FL
P_{IN} measurement range		$P_{IN(rng)}$	0		5500	W_{in}
P_{IN} measurement accuracy – standard measurement @ 25°C	> 450W < 450W	$\lvert P_{IN(acc)} \rvert$		45	+5 80	% W

[8]Clock, Data, and Alert# need to be pulled up to V_{DD} externally.

[9]Below 20% of FL; 10 – 20% of FL: ±0.82A; 5 – 10% of FL: ±0.60A; 2.5 – 5% of FL: ±0.42A.

[10]Above 2.5A of load current

[11]Within 30° of the default warning and fault levels.

Environmental Specifications

Parameter	Min	Typ	Max	Units	Notes
Ambient Temperature	-20[12]		60	°C	Measured at the maximum temperature of the mounting/cooling surface
Storage Temperature	-40		85	°C	
Operating Altitude			5000	m	
Non-operating Altitude			8200	m	
Power Derating with Temperature			1.0	%/°C	60°C to 75°C
Acoustic noise		0		dbA	Full load
Over Temperature Protection		125/110		°C	Shutdown / restart [internally measured points]
Humidity Operating Storage	 5 5		 95 95	 % %	Relative humidity, non-condensing
Shock and Vibration acceleration			2.4	Grms	IPC-9592B, Class II

[12]Designed to start and work at an ambient as low as -20°C, but may not meet operational limits until above -5°C

EMC

Parameter	Measurement	Standard	Level	Test
AC input[13]	Conducted emissions	EN55032, FCC Docket 20780 part 15, subpart J Meets Telcordia GR1089-CORE by a 3dB margin	A +6dB margin	0.15 – 30MHz
	Radiated emissions	EN55032	A +6dB margin	30 – 10000MHz
	Line harmonics	EN61000-3-2 THD	Table 1 5%	0 – 2 kHz 230 Vac, full load, 25°C

Parameter	Measurement	Standard	Criteria[14]	Test
AC Input Immunity	Line sags and interruptions	EN61000-4-11	B	-30%, 10ms
			B	-60%, 100ms
			B	-100%, 5sec
		Output will stay above 40V_{DC} @ 75% load Sag must be higher than 165Vrms.	A	25% line sag for 2 seconds 1 cycle interruption
	Lightning surge	EN61000-4-5, Level 4, 1.2/50µs – error free	A	4kV, common mode
			A	2kV, differential mode
		ANSI C62.41 - level A3	B	6kV, common & differential
	Fast transients	EN61000-4-4, Level 3	B	5/50ns, 2kV (common mode)
Enclosure immunity	Conducted RF fields	EN61000-4-6, Level 3	A	130dBµV, 0.15-80MHz, 80% AM
	Radiated RF fields	EN61000-4-3, Level 3	A	10V/m, 80-1000MHz, 80% AM
		ENV 50140	A	
	ESD	EN61000-4-2, Level 4	B	8kV contact, 15kV air

[13]Emissions requirements apply to rectifier with external filter to meet these requirements (see External EMI filter reference design).

[14]Criteria A: The product must maintain performance within specification limits. Criteria B: Temporary degradation which is self-recoverable. Criteria C: Temporary degradation which requires operator intervention.

Characteristic Curves

Characteristic curves will be provided for the following conditions.

Unless otherwise specified, the curves will reflect: 230V_{IN}, 55Vo, and 25°C temperature.

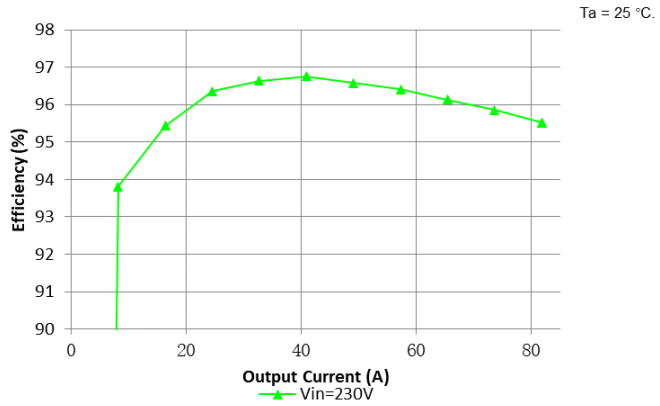


Fig 1 – Efficiency vs output current, Vo = 55V_{DC}, V_{IN} = 230V_{AC}

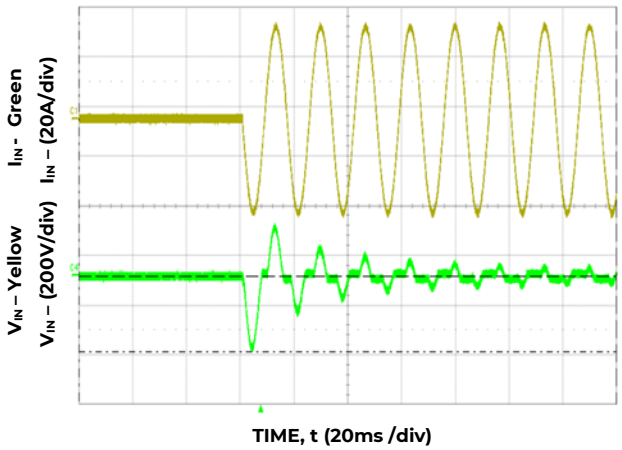


Fig 2 – Inrush current, V_{IN} = 277V_{AC}, 0 phase angle

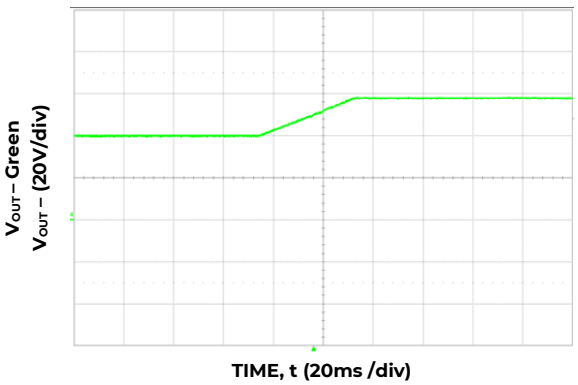


Fig 3 – Main output changed from 40V to 58V, commanded by I²C

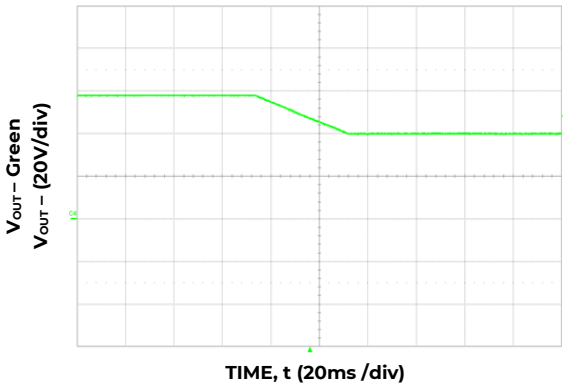


Fig 4 – Main output changed from 58V to 40V, commanded by I²C

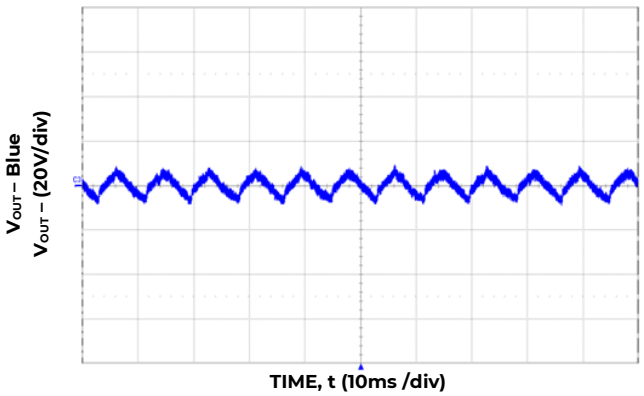


Fig 5 – Main output, ripple and noise, full load, V_{IN} = 185V_{AC}, 20MHz bandwidth

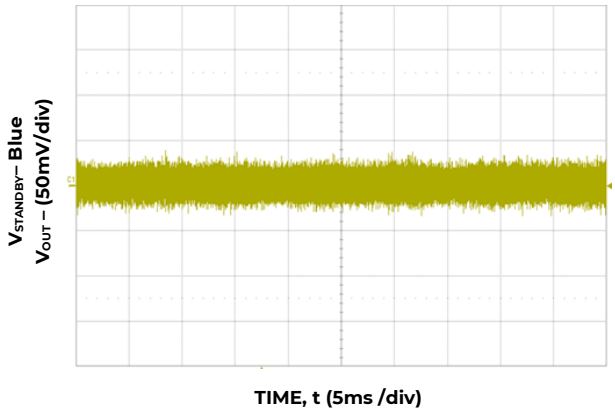


Fig 6 – Standby output, ripple and noise, full load, V_{IN} = 230V_{AC}, 20MHz bandwidth

Characteristic Curves (continued)

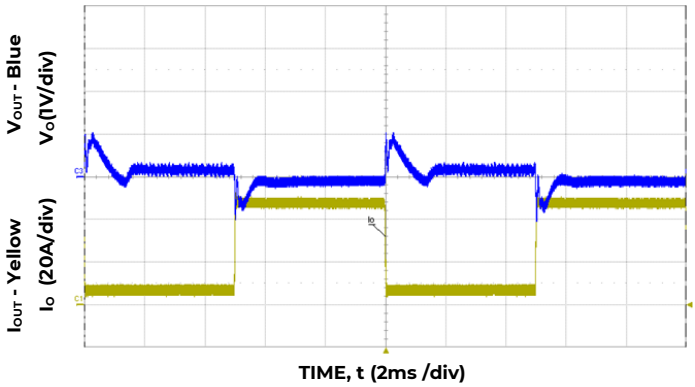


Fig 7 – Transient response, 10-60% load step, 1A/us 5ms high 5ms low, V_{IN} = 230V_{AC}

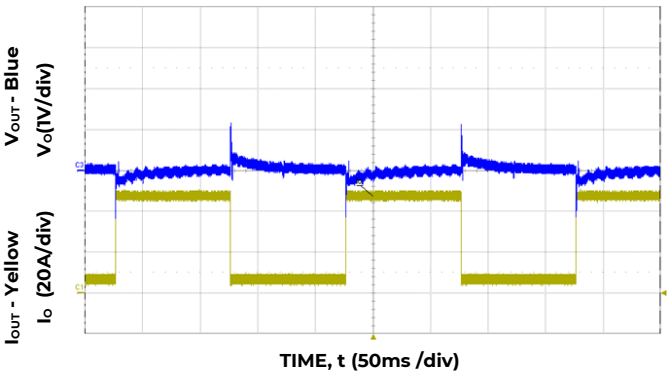


Fig 8 – Transient response, 10-60% load step, 1A/us 100ms high 100ms low, V_{IN} = 230V_{AC}

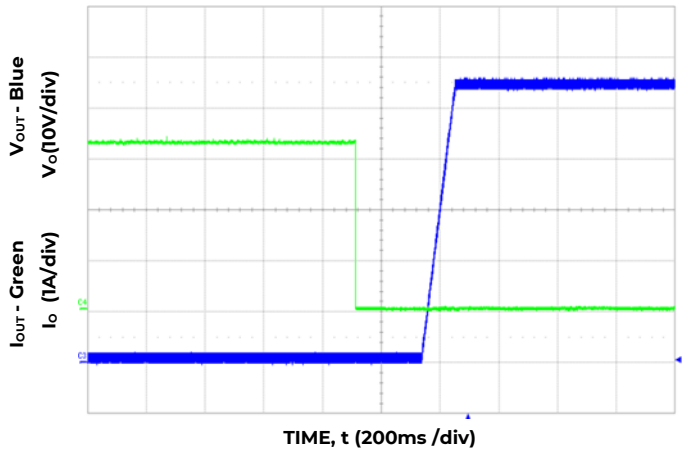


Fig 9 – Soft start delay and rise time when on/off is asserted, V_{IN} = 230V_{AC}, I²C mode

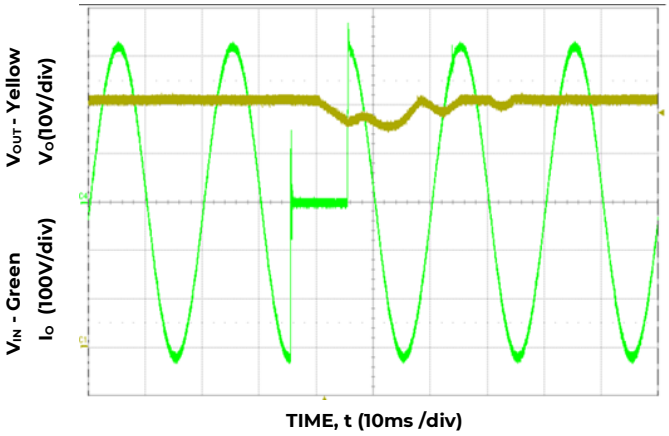


Fig 10– Ride through during 10ms , full load, V_{IN} = 230V_{AC}

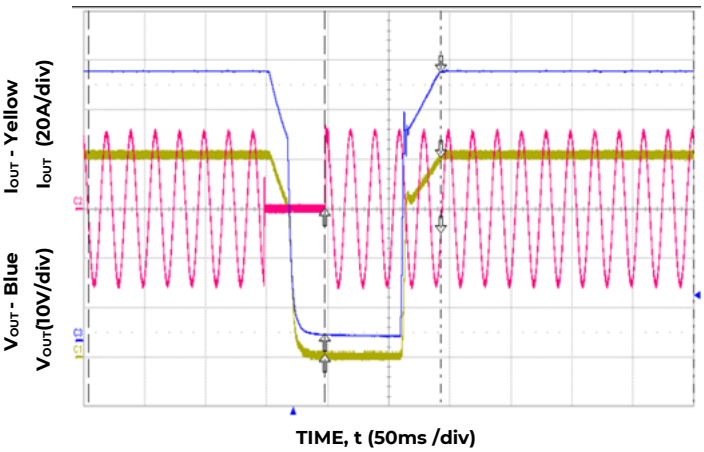


Fig 11 - 50ms AC drop-out at full load and V_{IN} = 230V_{AC}

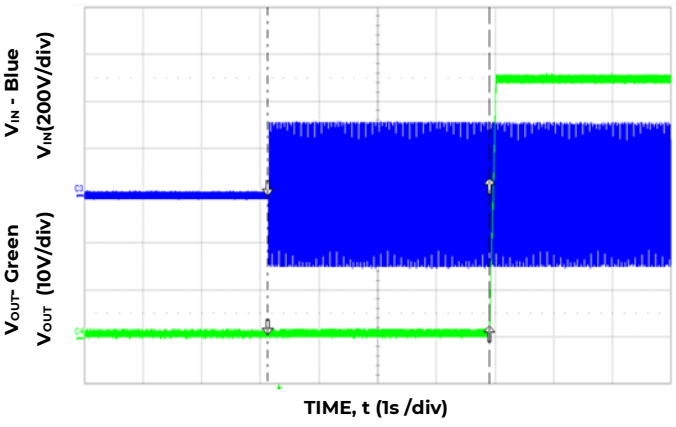


Fig 12 – Turn-on at full load and V_{IN} = 230V_{AC}

Characteristic Curves (continued)

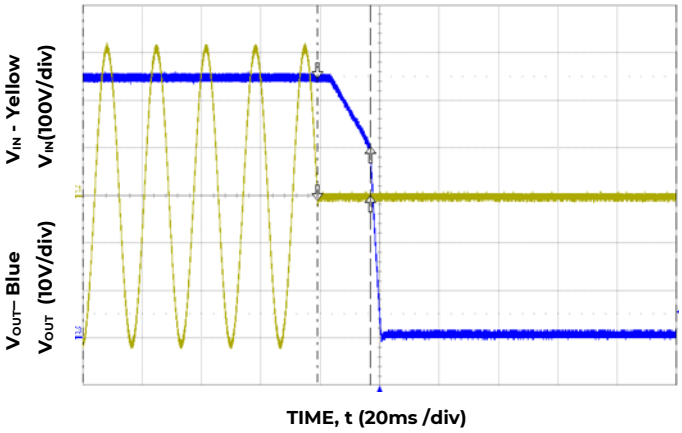


Fig 13 – Turn-off at full load, V_{IN} = 230V_{AC}

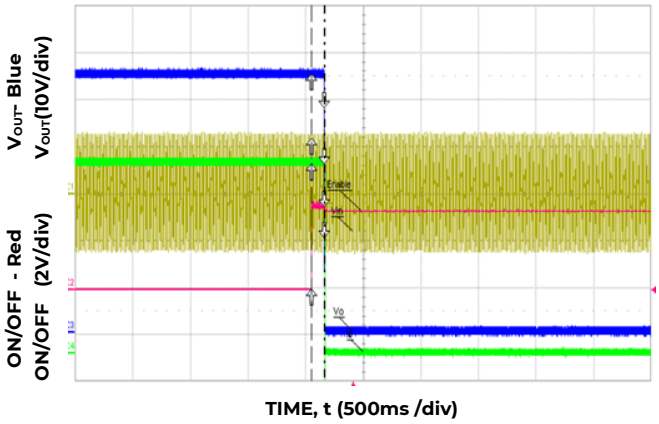


Fig 14 – Turn-off delay when on/off is de-asserted, 230V_{IN} and I²C mode

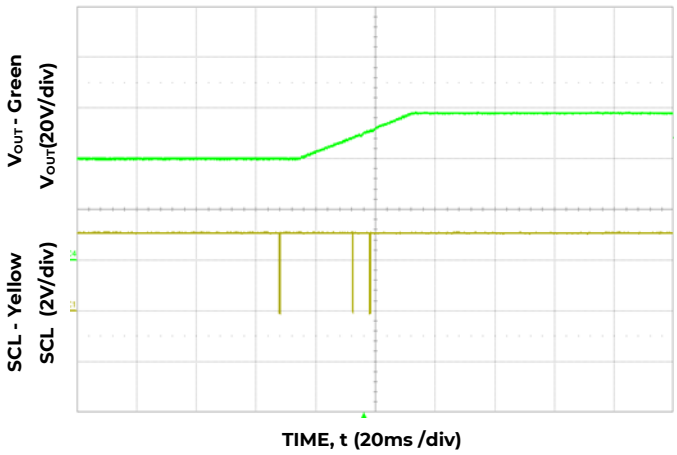


Fig 15 – Time delay from I²C command to output voltage changing

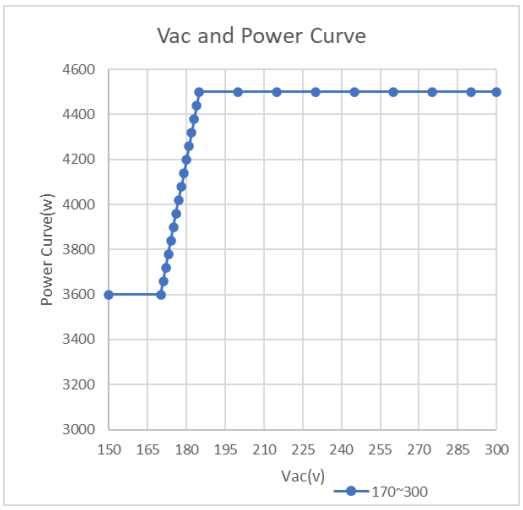


Fig 16 – Output derating vs input voltage below V_{IN} of 185V_{AC}

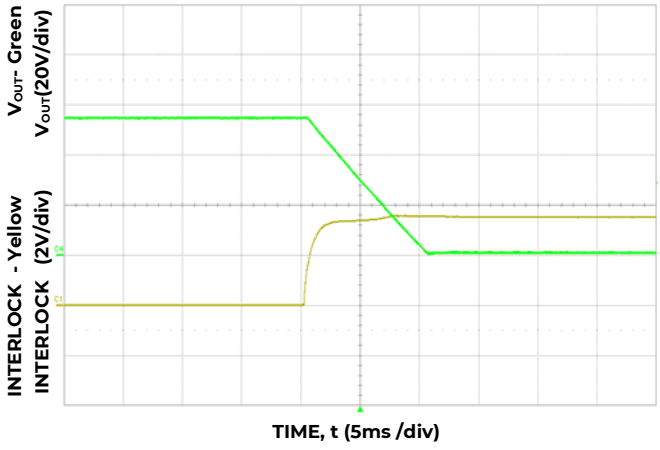
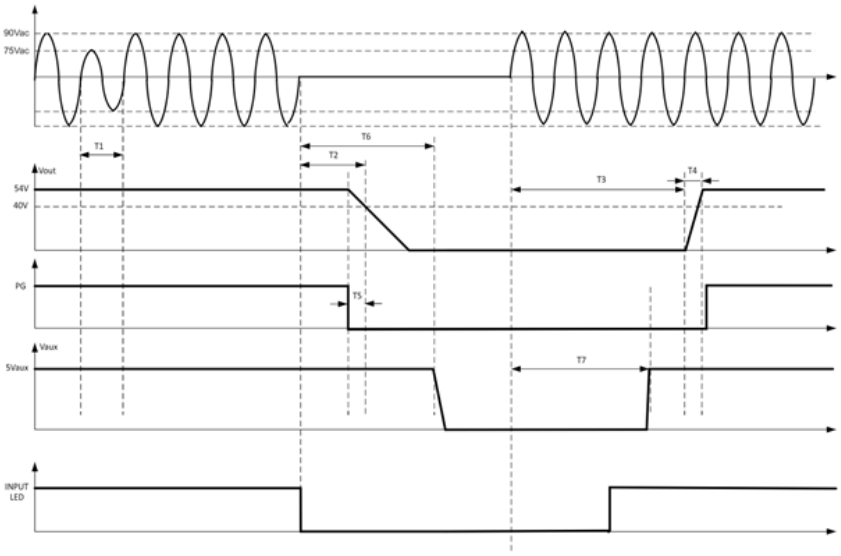


Fig 17 – Time delay from interlock reverse and output shut down. interlock signal can be used as quick turn off signal

Timing diagrams

This is the standard timing diagram for CC4500:



T1 – ride through time – 0.5 to 1 cycles [10 – 20ms] V_{OUT} remains within regulation – load dependent

T2 – hold up time – 15ms – V_{OUT} stays above $40V_{DC}$

T3 – delay time – 10s – from when the AC returns within regulation to when the output starts rising in I^2C mode

T4 – rise time – 120ms – the time it takes for V_{OUT} to rise from 10% to 90% of regulation in I^2C mode

T5 – power good warning – 3ms – the time between assertion of the PG signal and the output decaying below $40V_{DC}$.

T6 – hold up time of the 5VAUX output @ full load – 2s – from the time AC input failed

T7 – rise time of the 5VAUX output – 3.65ms – 5VAUX is available at least 450ms before the main output is within regulation

Blinking of the input/AC LED – $V_{IN} < 150V_{AC}$ (the low transitioned signal represents blinking of the input LED).

Fast Restart

A fast restart must occur after any AC outage as defined below. Fast restart is characterized by the power supply being in regulation (output back to 55V +/-2%), starting from AC back into nominal limits, in less than a specified time (faster than the normal start-up condition, as defined below), with the output rail being maintained at 51V by an auxiliary source (ultra-capacitor module) during the outage.

An AC outage is characterized by an AC voltage drop from nominal (steady within 170-300V) down to any voltage within 0V-170V for a duration longer than main output hold-up time, and as long as can handle the backup mechanism (ultra-capacitor).

Required fast restart time depends upon outage duration:

- For outages in 50ms, the power supply does not go in to shut down process, when the AC back, the output restart up immediately.
- For outages up to 800ms, maximum restart time is 150ms (see Figure 18).
- For outages ranging from 800ms up to 1.6s, maximum restart time is 450ms (Figure 19).
- For outages longer than 1.6s, there is no requirement regarding fast restart (normal start time can be used).

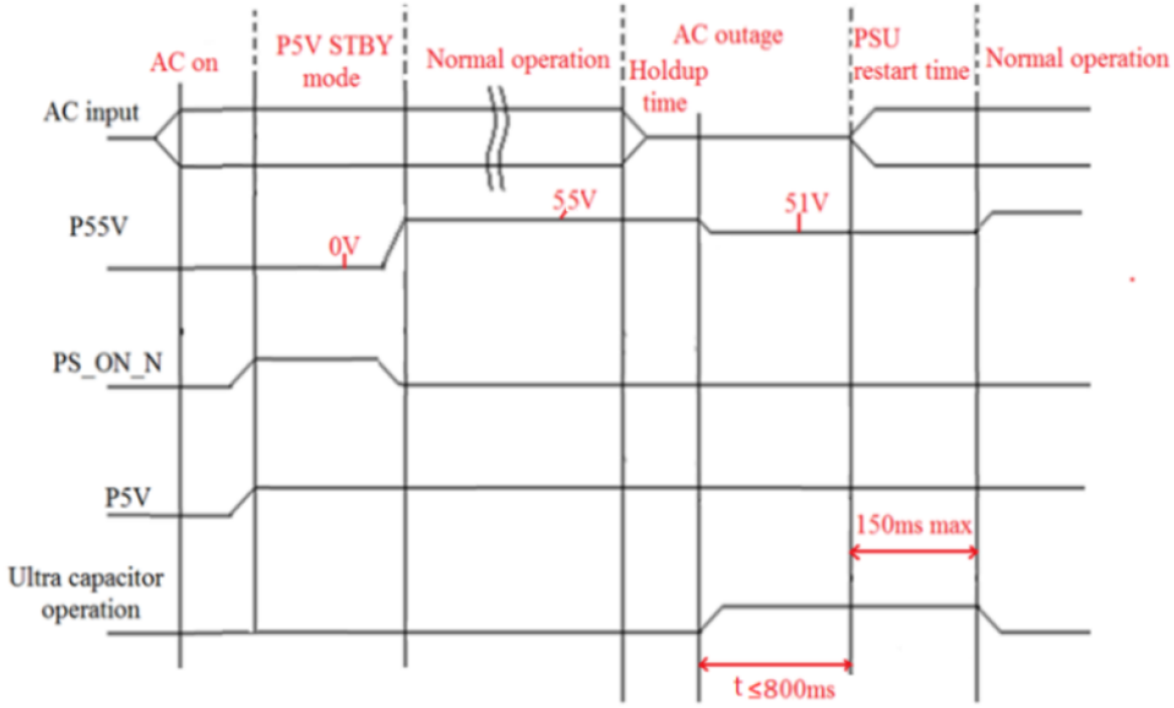


Fig 18 : Fast restart timings – outages shorter than 800ms

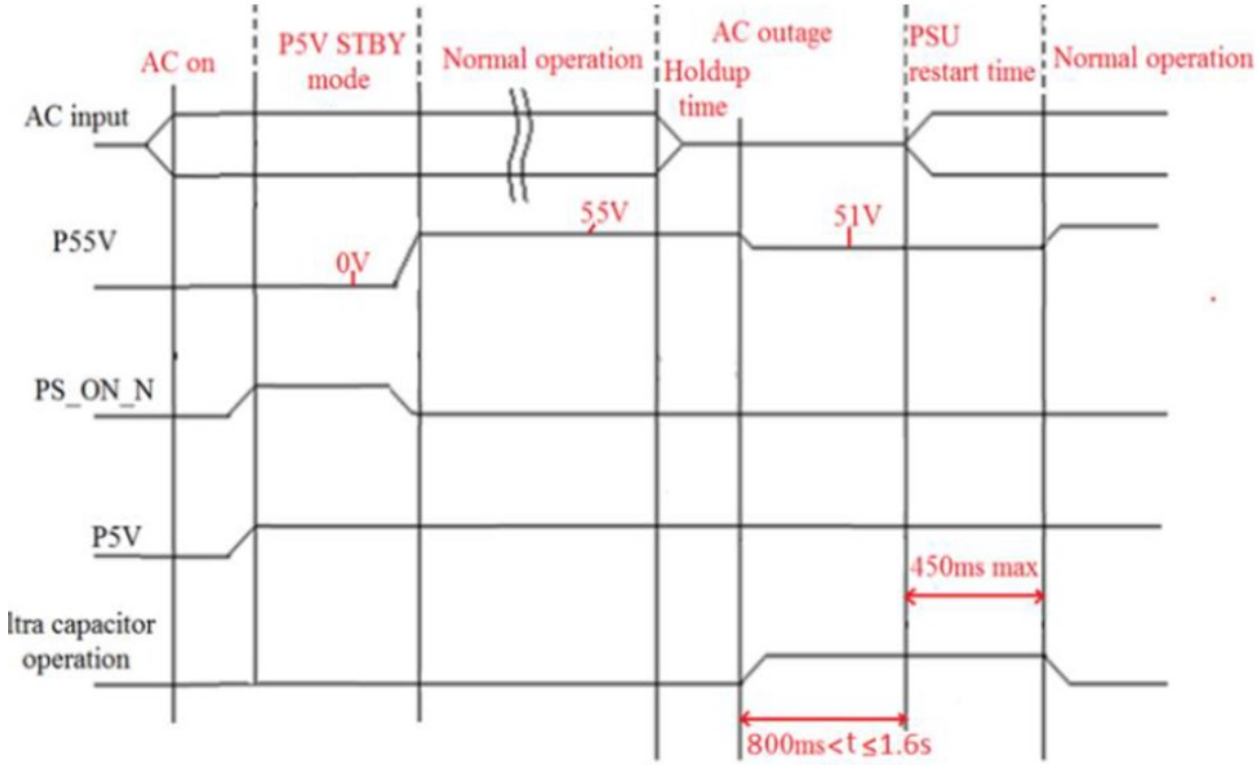


Fig 19 : Fast restart timings – outages between 800ms and 1.6s

Notes:

- For outages shorter than 300ms, the 150ms maximum restart time must be met whatever the load between 0 and 100% of full load.
- For outages from 300ms up to 800ms, the 150ms maximum restart time has to be met whatever the load between 0 and 50% of full load.
- For outages from 800ms up to 1.6s, the 450ms maximum restart time must be met whatever the load between 0 and 50% of full load.

In all the cases described above:

- The fast restart timing is to be met with 1 up to 36 PSUs operating in parallel.

The optional ultra-capacitor module connection is described below.

The boost converter powered by the charged Ultra capacitor is used to power the main DC rail when this one drops due to an AC outage and regulates the P55V output to 51V until 55V rail regains its nominal voltage (PSU restarts and provides the output power again).

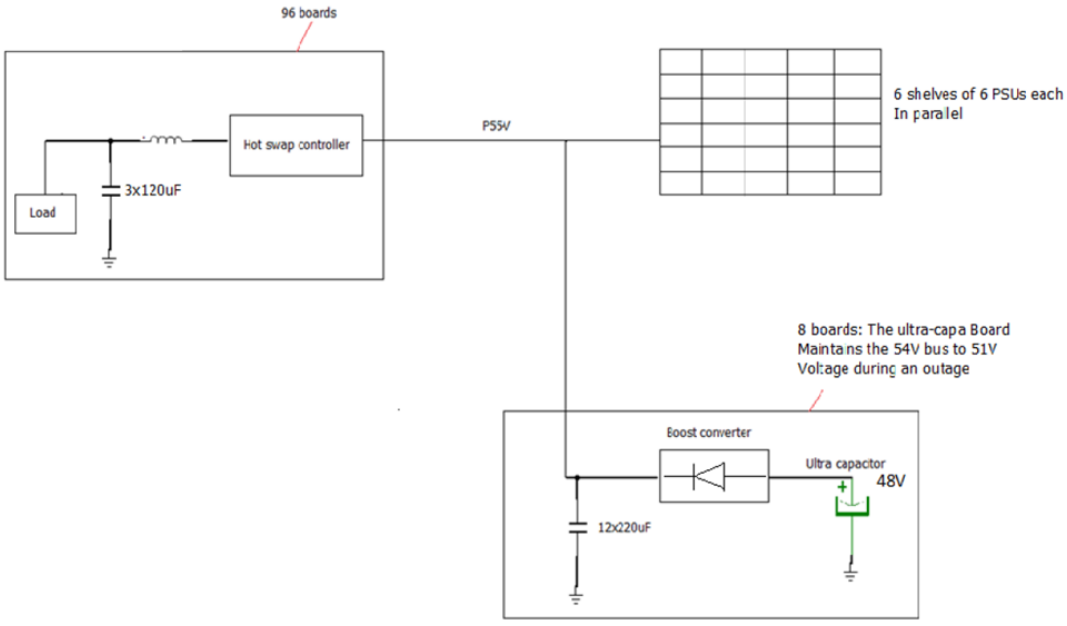


Fig 20 Ultra capacitor module connection

Maximum External Bulk Load Capacitance

- The power supply must be stable and meet all requirements with the following capacitive loading ranges.
- The total load capacitance of the system is expected to be from 0mF (min) to 56 instead of 35mF (max) on 55V power rail. On the 56mF, there will be 34.9mF protected by hot swap controller.
- (Worst case: one PSU starts with up to 56mF (with an equivalent ESR of 1mΩ) before the others).

Control and Status

The CC4500 provides three means for monitor/control: analog, PMBus™, or the OmniOn Galaxy-based RS485 protocol. Details of analog control and the PMBus™ based protocol are provided in this document. OmniOn provides separate application notes on the Galaxy RS485 based protocol for users to interface to the CC4500. Contact your local OmniOn representative for details.

Control Hierarchy

Some features, such as output voltage, can be controlled both through hardware and firmware. For example, the output voltage is controlled both by a signal pin (Vprog) and firmware (Vout_command, 0x21).

Using output voltage as an example, the Vprog signal pin voltage level sets the output voltage if its value is between 0.1 and 3.0 V_{DC} (see the "Voltage programming" section). When the programming signal Vprog is either a no-connect (0V), or between 0V and 0.1V the output voltage is set to 40V_{DC}. When the programming signal Vprog is >3.0V, the output voltage is set to 55V_{DC}.

The signal pin controls the corresponding feature until the firmware command is executed. Once the firmware command has been executed, the signal pin is ignored until input power is removed and reapplied, which resets control to the signal pin. In the above example, the CC4500 will no longer 'listen' to the Vprog pin after Vout_command has been executed, as long as input power is applied without interruption.

In summary, hardware signals such as Vprog are utilized for setting the initial default value and for varying the value until firmware based control takes over. Once firmware control is executed, hardware based control is relinquished so the processor can clearly decide who has control.

Analog Controls

Details of analog controls are provided in this document under Feature Specifications.

Signal Reference

Unless otherwise noted, all signals are referenced to Logic_GND ("Logic Ground"). See the Signal Definitions Table at the end of this document for further description of all the signals.

Logic_GND is isolated from the main output of the CC4500 for PMBus communications. Communications and the 5V standby output are not connected to main power return (Vout(-)) and can be tied to the system digital ground point selected by the user. (Note that RS485 communications is referenced to Vout(-), main power return of the CC4500).

Logic_GND is capacitively coupled to Earth Ground inside the CC4500 where Earth Ground is also wired to the metal case). The maximum voltage differential between Logic_GND and Earth Ground should be less than 100V_{DC}.

Delayed Overcurrent Shutdown during start-up

CC4500s are programmed to stay in a constant current state for up to 20 seconds during power up. This delay has been introduced to permit the orderly application of input power to a subset of paralleled front-ends during power up. If the overload persists beyond the 20 second delay, the front-end will revert to its programmed state of overload protection.

Unit in Power Limit or in Current Limit

When output voltage is > 40V_{DC} the Output LED will continue blinking. When output voltage is < 40V_{DC}, if the unit is in the RESTART mode, it goes into hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output LED is OFF. When the unit is in latched shutdown the output LED is OFF.

Auto Restart

Auto-restart is the default configuration for over-current and over-temperature shutdowns. These features are configured by the PMBus™ fault_ response commands.

An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again.

Restart after a latch-off

PMBus™ fault response commands can be configured to direct the CC4500 to remain latched off for overtemperature and overcurrent.

To restart after a latch off either of five restart mechanisms are available.

1. The hardware pin ON/OFF may be cycled OFF and then ON.
2. The unit may be commanded to restart via I²C through the Operation command by cycling the output OFF followed by ON.
3. Remove and reinsert the unit.
4. Turn OFF and then turn ON AC power to the unit.
5. Changing firmware from latch off to restart.

Each of these commands must keep the CC4500 in the OFF state for at least 2 seconds, with the exception of changing to restart. A successful restart shall clear all alarm registers, set the restarted successful bit of the Status_2 register.

A power system that is comprised of a number of CC4500s could have difficulty restarting after a shutdown event because of the non-synchronized behaviour of the individual CC4500s. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by:

Issuing a GLOBAL OFF and then ON command to all CC4500s, 2. Toggling Off and then ON the ON/OFF (ENABLE) signal 3. Removing and reapplying input commercial power to the entire system.

The CC4500s should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual CC4500s.

Control Signals

Protocol

This signal pin defines the communications mode setting of the CC4500. Two different states can be configured: State #1 is “Analog/PMBus” mode (I²C) for which the protocol pin should be left a no-connect. State #2 is the RS485 mode for which a resistor value between 1kΩ and 5kΩ should be present between this pin and Vout-.

Device Address in I²C mode

Address bits A3, A2, A1, A0 set the specific address of the microprocessor in the CC4500. With these four bits, up to sixteen (16) CC4500s can be independently addressed on a single I²C bus. These four bits are configured by two signal pins, Unit_ID and Rack_ID. The least significant bit x (LSB) of the address byte is set to either write [0] or read [1]. A write command instructs the CC4500. A read command accesses information from the CC4500.

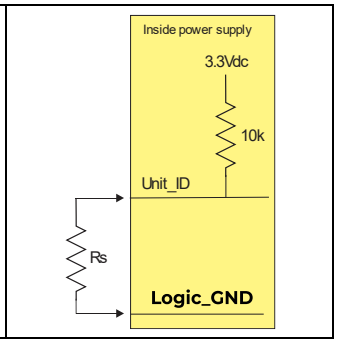
Device	Address	Address Bit Assignments (Most to Least Significant)							
		7	6	5	4	3	2	1	0
µP	40 – 4F	1	0	0	A3	A2	A1	A0	R/W
Broad cast	00	0	0	0	0	0	0	0	0
ARA[15]	C	0	0	0	1	1	0	0	1
		MSB							LSB

[15]Implement if feasible, this is a ‘read’ only address

Unit_ID

Up to 10 different units are selectable.

A voltage divider between 3.3V and Logic_GND configures Unit_ID. Internally a 10kΩ resistor is pulled up to $3.3V_{DC}$. A pull down resistor Rs needs to be connected between pin Unit_ID and Logic_GND .

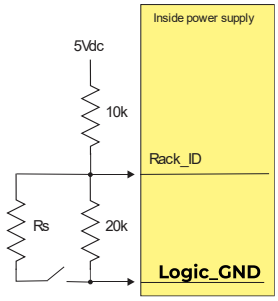


Unit_ID	Voltage level	R_S (± 0.1%)
Invalid	3.30	
1	3.00	100k
2	2.67	45.3k
3	2.34	24.9k
4	2.01	15.4k
5	1.68	10.5k
6	1.35	7.15k
7	1.02	4.99k
8	0.69	2.49k
9	0.36	1.27k
10	0	0

Rack_ID

Up to 8 different combinations are selectable.

A voltage divider between $5V_{DC}$ and Logic_GND configures Rack_ID. The 10k-20kΩ divider sets the initial voltage level to $3.3V_{DC}$. A switch between each R_S value changes the Rack_ID level according to the table below.



Rack_ID	Voltage level	R_S (± 0.1%)
1	3.3	open
2	2.8	35.2k
3	2.3	15k
4	1.8	8k
5	1.4	4.99k
6	1	2.87k
7	0.5	1.27k
8	0	0

Configuration of the A3 – A0 bits: The CC4500 will determine the configured address based on the Unit_ID and Rack_ID voltage levels as follows (the order is A3 – A0):

		Unit_ID				
		1	2	3	4	5
Rack_ID	1	0000	0001	0010	0011	
	2	0100	0101	0110	0111	
	3	1000	1001	1010	1011	
	4	1100	1101	1110	1111	
	5					
	6	0000	0001	0010	0011	0100
	7	0101	0110	0111	1000	1001
	8	1010	1011	1100	1101	1110

Unit x Rack: 4 x 4 and 5 x 3

		Unit_ID				
		6	7	8	9	10
Rack_ID	1	0000	0001			
	2	0010	0011			
	3	0100	0101			
	4	0110	0111	0000	0001	0010
	5	1000	1001	0011	0100	0101
	6	1010	1011	0110	0111	1000
	7	1100	1101	1001	1010	1011
	8	1110	1111	1100	1101	1110

Unit x Rack: 2 x 8 and 3 x 5

Address Detection

The Slot_ID pin must be connected to Vout- in order to deliver output power. This connection provides a second interlock feature. This connection may be a short circuit or any resistance up to 100 kohm, to allow addressing in RS485 mode as described below.

Device Address in RS485 mode

The address in RS485 mode is divided into three components: Bay_ID, Slot_ID and Shelf_ID.

Bay_ID: The Unit_ID definition in I^2C mode becomes the bay id in RS485 mode.

Slot_ID: Up to 10 different CC4500s could be positioned across a shelf. The resistor below needs to be placed between Slot_ID and Vout-. Internal pull-up to 3.3V is 10kΩ.

Slot	Resistor	Voltage	Slot	Resistor	Voltage
invalid	none	3.3V	6	7.15k	1.35V
1	100k	3V	7	4.99k	1.02V
2	45.3k	2.67V	8	2.49k	0.69V
3	24.9k	2.34V	9	1.27k	0.36V
4	15.4k	2.01V	10	0	0
5	10.5k	1.68V			

Shelf_ID: When placed horizontally up to 10 shelves can be stacked on top of each other in a fully configured rack. The shelf will generate the precision voltage level tabulated below referenced to Vout-.

Shelf	V_{MIN}	V_{NOM}	V_{MAX}
1	2.3	2.5	2.7
2	4.7	5.0	5.3
3	7.4	7.5	7.6
4	9.5	10.0	10.5
5	11.8	12.5	13.2
6	14.2	15.0	15.8
7	16.6	17.5	18.4
8	19	20.0	21
9	21.3	22.5	23.6
10	23.8	25.0	26.3

Global Broadcast

This is a powerful command because it instruct all CC4500s to respond simultaneously. A read instruction should never be accessed globally. The CC4500 should issue an 'invalid command' state if a 'read' is attempted globally.

For example, changing the 'system' output voltage requires the global broadcast so that all paralleled CC4500s change their output simultaneously. This command can also turn OFF the 'main' output or turn ON the 'main' output of all CC4500s simultaneously. Unfortunately, this command does have a side effect. Only a single CC4500 needs to pull down the ninth acknowledge bit. To be certain that each CC4500 responded to the global instruction, a READ instruction should be executed to each CC4500 to verify that the command properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

Alert Response Address (ARA)

This feature enables the 'master' to rapidly determine which 'slave' CC4500 triggered.

the Alert# signal without having to poll each CC4500 one at a time. During normal operation, the CC4500 activates (pulls down LO) the Alert# signal line indicating that it needs attention when a 'state' change occurs. The master can determine who pulled the 'alert' line by sending out the alert-response-address, address 12b, with a 'read' instruction. If the CC4500 triggered the 'alert' it should respond back with its address. The instruction takes the form below:

1	8		1	8	1	8	1	1
S	ARA	Rd	A	My	A	PEC	A	P

If during the ARA response multiple CC4500s send out their addresses, then the actual address received by the master is the lowest address from the combinations of those CC4500s that responded.

The 'my address' field contains the address of the CC4500 in the 7 most significant bits (msb) of the byte. The lsb of the byte is a don't care, it could be a 0 or a 1. For more information refer to the SMBus specification.

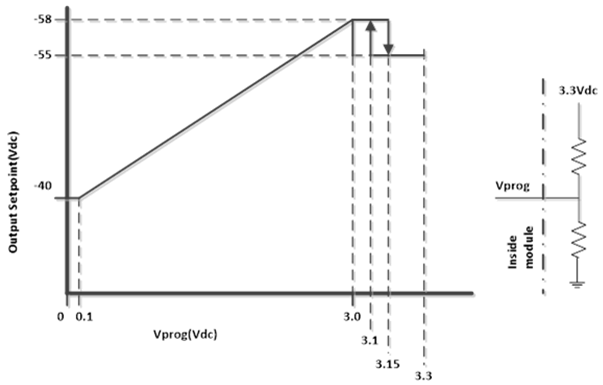
The micro-controller needs to read the actual my address data byte that is sent back to the master. If the my-address data byte agrees with the address of this unit, then, and only then, the microcontroller needs to clear (de-assert) its Alert# signal. Thus, the CC4500 whose address has been sent out gets de-asserted from the joint Alert# line.

If the Alert# line is still asserted, the host should send out an ARA request again and find out who else asserted Alert#. This process needs to continue until the Alert# is released which is a clear indication that all CC4500s that asserted Alert# have had their status states read back.

Voltage Programming (Vprog)

Hardware voltage programming controls the output voltage until a software command to change the output voltage is executed. Then software voltage programming overrides the hardware margin setting and the CC4500 no longer listens to any hardware margin settings until power to the controller is interrupted, for example if input power or bias power is cycled off, then on.

Under hardware voltage programming, an analog voltage on Vprog can vary the output voltage linearly from $40V_{DC}$ to $58V_{DC}$ for 0.1V ≤ Vprog ≤ 3.0V referenced to Logic_GND. If Vprog is raised ≥3.15V, Vout is set to its default value of 55V. If 0 ≤ Vprog <0.1V, Vout is set to 40V



The Vprog pin level can be set by an external resistor divider between an external voltage source and Logic_GND as shown in the figure above, or by a precision voltage source connected between Vprog and Logic_GND.

When bias power to the controller is recycled, the controller restarts into its default configuration, programmed to set the output voltage as instructed by the Vprog pin. Again, subsequent software commanded settings permanently override the “Vout Adjust” setting.

Before enabling a hot-plugged CC4500, the output voltage should be set to a safe level - no higher than the bus voltage to avoid a transient or possible shutdown. Assuming the shelf enables the CC4500 by shorting ON/OFF to Logic_GND , the shelf should also pull Vprog to a safe level. This could be 3.3V, setting Vout to 55V. The hot-plugged CC4500 will remain at this output voltage, possibly supplying no power, until commanded to a higher voltage.

Load Share (Ishare)

This is a single wire analog signal that is generated and acted upon automatically by CC4500s connected in parallel. Ishare pins should be connected to each other for CC4500s, if active current share among the CC4500s is desired. No resistors or capacitors should get connected to this pin.

On/Off

Controls the main $55V_{DC}$ output when either analog control or PMBus protocols are selected, as configured by the Protocol pin. This pin must be pulled low to turn ON the CC4500. The CC4500 will turn OFF if either the ON/OFF or the Interlock pin is released. This signal is referenced to Logic_GND. Note that in RS485 mode the ON/OFF pin is ignored.

Interlock

This is a shorter pin utilized for hot-plug applications to ensure that the CC4500 turns OFF before the power pins are disengaged. It also ensures that the CC4500 turns ON only after the power pins have been engaged. Must be connected to VOUT- for the CC4500 to be ON.

Module Present

This signal is tied to Logic_GND inside the CC4500. Its intent is to provide a signal to the system that a CC4500 is physically present in the slot.

8V_int

Single wire connection between CC4500s, Provides bias to the DSP of an unpowered CC4500. This is not intended for customer use.

Status Signals

Power Good Warning (PG#)

This signal is HI when the main output is being delivered and goes LO if the main output is about to decay below regulation. Note that should a catastrophic failure occur, the signal may not be fast enough to provide a meaningful warning. PG# also pulses at a 1ms duty cycle if the unit is in overload.

Fault#

A TTL compatible status signal representing whether a Fault occurred. This signal needs to be pulled HI externally through a resistor. This signal goes LO for any failure that requires CC4500 replacement. These faults may be due to:

- Over-temperature shutdown
- Over-voltage shutdown
- Internal CC4500 Fault

Over temperature warning (OTW#)

A TTL compatible status signal representing whether an over temperature exists. This signal needs to be pulled HI externally through a resistor.

If an over temperature should occur, this signal would pull LO for approximately 10 seconds prior to shutting down the CC4500. In its default configuration, the unit would restart if internal temperatures recovered within normal operational levels. At that time, the signal reverts to its open collector (HI) state.

Serial Bus Communications

The I²C interface facilitates the monitoring and control of various operating parameters within the unit and transmits these on demand over an industry standard I²C Serial bus. All signals are referenced to 'LOGIC_GND '.

Pull-up resistors

The clock, data, and Alert# lines do not have any internal pull-up resistors inside the CC4500. The customer is responsible for ensuring that the transmission impedance of the communications lines complies with I²C and SMBus standards.

Serial Clock (SCL)

The clock pulses on this line are generated by the host that initiates communications across the I²C Serial bus. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I²C /SMBus specifications.

Serial Data (SDA)

This line is a bi-directional data line. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I²C /SMBus specifications.

Digital Feature Descriptions

PMBus Compliance:

The CC4500 is fully compliant to the Power Management Bus (PMBus™) rev1.2 requirements. This Specification can be obtained from **www.pmbus.org**.

'Manufacturer Specific' commands are used to support additional instructions that are not in the PMBus™ specification.

All communication over the PMBus interface must support the Packet Error Checking (PEC) scheme. The PMBus master must generate the correct PEC byte for all transactions, and check the PEC byte returned by the CC4500.

The Alert# response protocol (ARA) whereby the PMBus Master can inquire who activated the Alert# signal is also supported. This feature is described in more detail later on.

Non-volatile memory is used to store configuration settings. Not all settings programmed into the device are automatically saved into this non-volatile memory. Only those specifically identified as capable of being stored can be saved. (see the Table of Commands for which command parameters can be saved to non-volatile storage).

Non-supported Commands

Non-supported commands are flagged by setting the appropriate STATUS bit and issuing an Alert# to the 'host' controller. If a non-supported read is requested the CC4500 will return 0x00h for data.

Data out-of-range

The CC4500 validates data settings and sets the data out-of-range bit and Alert# if the data is not within acceptable range.

Master/Slave

The 'host controller' is always the MASTER. CC4500s are always SLAVES. SLAVES cannot initiate communications or toggle the Clock. SLAVES also must respond expeditiously at the command of the MASTER as required by the clock pulses generated by the MASTER.

Clock Stretching

The 'slave' microcontroller inside the CC4500 may initiate clock stretching if it is busy and it desires to delay the initiation of any further communications. During the clock stretch the 'slave' may keep the clock LO until it is ready to receive further instructions from the host controller. The maximum clock stretch interval is 25ms.

The host controller needs to recognize this clock stretching, and refrain from issuing the next clock signal, until the clock line is released, or it needs to delay the next clock pulse beyond the clock stretch interval of the CC4500. Note that clock stretching can only be performed after completion of transmission of the 9th ACK bit, the exception being the START command.

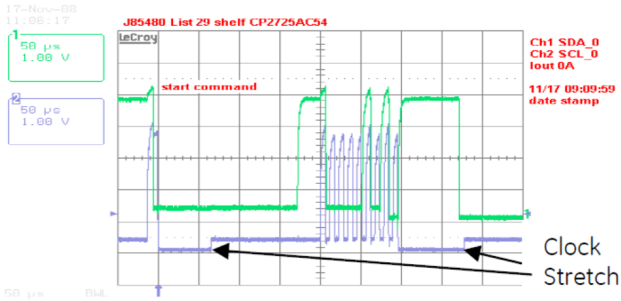


Fig 21 Example waveforms showing clock stretching

I²C Bus Lock-up detection

The device will abort any transaction and drop off the bus if it detects the bus being held low for more than 35ms.

Communication speed

Both 100kHz and 400kHz clock rates are supported. Default is at 100kHz.

Packet Error Checking (PEC)

The CC4500 will not respond to commands without the trailing PEC. The integrity of communications is compromised if packet error correction is not employed. There are many functional features, including turning OFF the main output, that require validation to ensure that the desired command is executed.

PEC is a CRC-8 error-checking byte, based on the polynomial $C(x) = x^8 + x^2 + x + 1$, in compliance with PMBus™ requirements. The calculation is based in all message bytes, including the originating write address and command bytes preceding read instructions. The PEC is appended to the message by the device that supplied the last byte.

Alert#

The CC4500 can issue Alert# driven from either its internal micro controller or from the I²C bus master selector stage. That is, the Alert# signal of the internal microcontroller funnels through the master selector stage that buffers the Alert# signal and splits the signal to the two Alert# signal pins exiting the CC4500. In addition, the master selector stage signals its own Alert# request to either of the two Alert# signals when required.

The microcontroller driven Alert# signal informs the 'master/host' controller that either a STATE or ALARM change has occurred. Normally this signal is HI. The signal will change to its LO level if the CC4500 has changed states and the signal will be latched LO until the CC4500 receives a 'clear_faults' instruction.

The signal will be triggered for any state change, including the following conditions:

- V_{IN} under or over voltage
- V_{OUT} under or over voltage
- I_{OUT} over current
- Over Temperature warning or fault
- Communication error
- PEC error
- Invalid command
- Internal faults

Both Alert# -0 and -1 are asserted during power up to notify the master that a new CC4500 has been added to the bus.

The CC4500 will clear the Alert# signal (release the signal to its HI state) upon the following events:

- Receiving a CLEAR_FAULTS command
- Bias power to the processor is recycled

The CC4500 will re-assert the Alert line if the internal state of the CC4500 has changed, even if that information cannot be reported by the status registers until a clear_faults is issued by the host. If the Alert asserts, the host should respond by issuing a clear_faults to retire the alert line (this action also provides the ability to change the status registers). This action triggers another Alert assertion because the status registers changed states to report the latest state of the CC4500. The host is now able to read the latest reported status register information and issue a clear_faults to retire the Alert signal.

Re-initialization

The I²C code is programmed to re-initialize if no activity is detected on the bus for 5 seconds. Re-initialization is designed to guarantee that the I²C microcontroller does not hang up the bus. Although this rate is longer than the timing requirements specified in the SMBus specification, it had to be extended in order to ensure that a re-initialization would not occur under normal transmission rates. During the few microseconds required to accomplish re-initialization the I²C microcontroller may not recognize a command sent to it. (i.e. a start condition).

Read-back delay

The CC4500 issues the Alert# notification as soon as the first state change occurred. During an event, a number of different states can be transitioned to before the final event occurs. If a read-back is implemented rapidly by the host a successive Alert# could be triggered by the transitioning state of the CC4500. In order to avoid successive Alert# s and read -backs and also to avoid reading a transitioning state, it is prudent to wait more than 2 seconds after the receipt of an Alert# before executing a read-back. This delay will ensure that only the final state of the CC4500 is captured.

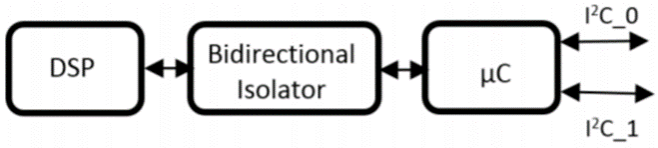
Successive read-backs

Successive read-backs to the CC4500 should not be attempted at intervals faster than every one second. This time interval is sufficient for the internal processors to update their data base so that successive reads provide fresh data.

Dual redundant buses

Two independent I²C lines provide true communications bus redundancy and allow two independent controllers to sequentially control the CC4500. For example, a short or an open connection in one of the I²C lines does not affect communications capability on the other I²C line. Failure of a 'master' controller does not affect the CC4500s and the second 'master' can take over control at any time.

Conceptually a Digital Signal Processor (DSP) referenced to Vout- of the CC4500 provides secondary control. A Bidirectional Isolator provides the required isolation between power ground, Vout- and signal/ logic ground (LOGIC_GND). A secondary microcontroller provides instructions to and receives operational data from the DSP. The secondary microcontroller also controls the communications over two independent buses.



The secondary micro controller is designed to default to I²C_0 when powered up. If only a single system controller is utilized, it should be connected to I²C_0. In this case the I²C_1 line is totally transparent as if it does not exist.

If two independent system controllers are utilized, then one of them should be connected to I²C_0 and the other to I²C_1.

At power up, the master connected to I²C_0 has control of the bus. See the section on Dual Master Control for further description of this feature.

PMBus Commands

Standard Instruction

Up to two bytes of data may follow an instruction depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

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1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1	8	1	1
Low data byte	A	High data byte	A	PEC	A	P

Master to Slave Slave to Master
SMBUS annotations: S – Start , Wr – Write, Sr – re-Start, Rd – Read,
A – Acknowledge, NA – not-acknowledged, P – Stop

Standard Read

Up to two bytes of data may follow a READ request depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	7	1	1	8	1
Sr	Slave address	Rd	A	LSB	A

8	1	8	1	1
MSB	A	PEC	NA	P

Block communications

When writing or reading more than two bytes of data at a time BLOCK instructions for WRITE and READ commands are used instead of the Standard Instructions above to write or read any number of bytes greater than two.

Block write format:

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1	8		1
Byte count = N	A	Data 1	A	Data 2		A

8	1	8	1	8	1	1
.....	A	Data N	A	PEC	A	P

Block Read format:

1	7	1	1		8	1
S	Slave address	Wr	A		Command Code	A

1	7	1	1
Sr	Slave address	Rd	A

8	1	8	1	8		1
Byte count = N	A	Data 1	A	Data 2		A

8	1	8	1	8	1	1
.....	A	Data N	A	PEC	NA	P

Linear Data Format

The definition is identical to Part II of the PMBus Specification. All standard PMBus values, with the exception of output voltage related functions, are represented by the linear format described below. Output voltage functions are represented by a 16 bit mantissa. Output voltage has a E=9 constant exponent.

The Linear Data Format is a two byte value with an 11-bit, two's complement mantissa and a 5-bit, two's complement exponent or scaling factor, its format is shown below.

	Data Byte High								Data Byte Low							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Exponent (E)								Mantissa (M)							

The relationship between the Mantissa, Exponent, and Actual Value (V) is given by the following equation:

$$V = M * 2^{E}$$

Where: V is the value, M is the 11-bit, two's complement mantissa, E is the 5-bit, two's complement exponent.

Standard Features

Supported Features that are not readable

The commands below are supported at the described setting but they cannot be read back through the command set.

Command	Comments
ON_OFF_CONFIG (0x02)	Both the CNTL pin, and the OPERAION command, enabling ordisabling the output, are sup- ported. Other options are not supported
Capability (0x19)	400KHz, ALERT#
PMBus revision (0x98)	1.2

Status and Alarm Registers

The registers are updated with the latest operational state of the CC4500. For example, whether the output is ON or OFF is continuously updated with the latest state of the CC4500. However, alarm information is maintained until a clear_faults command is received from the host. For example, the shutdown or OC_fault bits stay in their alarmed state until the host clears the registers.

A clear_faults clears all registers. If a fault still persists after the clear_faults is commanded, the register bit annunciating the fault is reset again.

Adjustment Ranges & Default Values for PMBUS in case of CC4500AC55FB

Some of the PMBus commands on the next page enable adjustment of operating parameters within the ranges specified below. If a command is received with a value outside this range, the module does not change the present setting. Instead it uses CML to indicate a communication failure.

Command	Hex Code	Default	Adjustment range	
			Low	High
Vout_command	0x21	55	40	58
Vout_OV_fault_ limit	0x40	60	42	63
Vout_OV_warn_ limit	0x42	59	42	63
Vout_UV_warn_ limit	0x43	52	35	58
Vout_UV_fault_limit	0x44	38	35	58
Iout_OC_fault_limit	0x46	88	10	88
Iout_OC_LV_fault_ limit	0x48	35	5	35
Iout_OC_warn_ limit	0x4A	86.5	01	90
OT_fault_limit	0x4F	100	70	150
OT_warn_limit	0x51	95	70	150
Vin_OV_warn_limit	0x57	295	185	305
Vin_UV_warn_limit	0x58	170	70	265
IIN_OC_WARN	0x5D	30	10	40
Mfr_ID	0x99	ATOS		
Mfr_model	0x9A	CC4500AC55FB		
T-time	0xF4	3	1	150
IOUT_OC_TRIG_ ENABLE	0xF5	Disable	1 is Enable and 0 is Disable	
IOUT_OC_CAP_ LIMIT	0xF6	100	0	110
ASSERTION_TIME	0xF7	250	100	300

To be updated:

PMBus™ fault_response commands exact default values will be updated after Atos tests. Current hypothesis is latch off for all faults (Vout OV, Vout UV, Iout OC, Vin OV), except for OTP and Vin UV for which automatic restart is required.

Command Descriptions

Commands are listed in numerical order, with a summary table at the end of this section.

Operation (0x01)

Turns the 55V output ON or OFF. The default state is ON at power up. Only the following data bytes are supported:

FUNCTION	DATA BYTE
Unit ON	0x80
Unit OFF	0x00

To RESET the CC4500 using this command, command the CC4500 OFF, wait at least 2 seconds, and then command the CC4500 back ON. All alarms and shutdowns are cleared during a restart.

Clear_Faults (0x03)

Clears all STATUS and FAULT registers and resets the Alert# line of the I²C side in control. The I²C side not in control cannot clear registers in the CC4500. This command is always executable.

If a fault persists after the issuance of the clear_faults command, the specific registers indicating the fault first clears but then get set again to indicate that the unit is still in the fault state.

Write_Protect register (0x10)

Used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. All supported commands may have their parameters read, regardless of the write_protect settings. The contents of this register cannot be stored into non-volatile memory using the Store_user_code command. The default setting of this register is enable_all_writes, write_protect 0x00h. The write_protect command must always be accepted.

FUNCTION	DATA BYTE
Enable all writes	00
Disable all writes except write_protect	80
Disable all writes except write_protect and OPERATION	40

Restore_Default_All (0x12)

Restores all operating register values and responses to the factory default parameters set in the CC4500. The factory default cannot be changed.

Restore_default_code (0x14)

Restore only a specific register parameter into the operating register section of the CC4500.

Store_user_code (0x17)

Changes the user default setting of a single register. In this way, some protection is offered to ensure that only those registers that are desired to be changed are in fact changed.

Restore_user_code (0x18)

Restores the user default setting of a single register.

Vout_mode (0x20)

This is a 'read only' register. The upper three bits specify the supported data format, in this case Linear mode. The lower five bits specify the exponent of the data in two's complement binary format for output voltage related commands, such as Vout_command. These commands have a 16 bits mantissa. The exponent is fixed by the CC4500 and is returned by this command.

Mode	Bits [7:5]	Bits [4:0] (Parameter)
Linear	000b	xxxxxb

Vout_Command (0x21)

This is used to dynamically change the output voltage of the CC4500. This command can also be used to change the factory programmed default set point of the CC4500 by executing a store-user instruction that changes the user default firmware set point.

The default set point can be overridden by the Vprog signal pin which is designed to override the firmware based default setting during turn ON.

In parallel operation, changing the output voltage should be performed simultaneously to all CC4500s using the Global Address (Broadcast) feature. If only a single CC4500 is instructed to change its output, it may attempt to source all the required power which can cause either a power limit or shutdown condition.

Digital programming of output voltage overrides the set point voltage configured by the Vprog signal pin as long as ac input power is applied continuously. The program no longer looks at the 'Vprog pin' and will not respond to any hardware voltage settings. If ac input power is removed, the microcontroller is reset to its default configuration, looking at the Vprog signal for output voltage control. In many applications, the Vprog pin is used for setting initial conditions, if different that the factory setting. Software programming then takes over once a Vout_Command is sent.

To properly hot-plug a CC4500 into a live backplane, the system generated voltage should match either the factory adjusted firmware level or the voltage level reconfigured by the Vprog pin. Otherwise, the voltage state of the plugged in CC4500 could be significantly different than the powered system.

Programmed voltage range: 40V_{DC} – 58V_{DC}.

A voltage programming example: The task: set the output voltage to 50.45V_{DC}. This CC4500 supports the linear mode of conversion specified in the PMBus™ specification. The supported output voltage exponent is documented in the Vout_mode (0x20) command. The exponent for output voltage setting is 2-9 (see the PMBus™ specification for reading this command). Calculate the required voltage setting to be sent: 50.45 x 29 = 25830. Convert this decimal number into its hex equivalent: 64E6 and send it across the bus LSB first and then MSB; E664 with the trailing PEC.

Vin_ON (0x35)

This is a 'read only' register that informs the controller at what input voltage level the CC4500 turns ON. The default value is tabulated in the data section.

Vin_OFF (0x36)

This is a 'read only' register that informs the controller at what input voltage level the CC4500 turns OFF. The default value is tabulated in the data section.

Vout_OV_fault_limit (0x40)

Sets the value at which the main output voltage will shut down. The default OV_fault value is set at 60V_{DC}. This level can be permanently changed and stored in non-volatile memory.

Vout_OV_fault_response (0x41)

This is a 'read only' register. The only allowable state is a latched state after three retry attempts.

An overvoltage shutdown is followed by three attempted restarts, each successive restart delayed 1

second. If within a 1 minute window, three attempted restarts failed, the unit will latch OFF. If less than 3 shutdowns occur within the 1 minute window then the count for latch OFF resets and the 1 minute window starts all over again. This performance cannot be changed.

Restart after a latched state: Either of four restart mechanisms is available:

- The hardware pin **ON/OFF** may be cycled OFF and then ON.
- The unit may be commanded to restart via I^2C through the Operation command by first turning OFF then turning ON.
- The third way to restart is to remove and reinsert the unit.
- The fourth way is to turn OFF and then turn ON ac power to the unit.

A successful restart clears all STATUS and ALARM registers.

A power system that is comprised of a number of CC4500s could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual CC4500s. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

- Issuing a GLOBAL OFF and then a GLOBAL ON command to all CC4500s
- Toggling Off and then ON the **ON/OFF** signal, if this signal is paralleled among the CC4500s.
- Removing and reapplying input commercial power to the entire system.

The CC4500s should be OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual CC4500s.

Vout_OV_warn_limit (0x42)

Sets the value at which a warning will be issued that the output voltage is too high. The default OV_warn limit is set at $59V_{DC}$. Exceeding the warning value will set the Alert# signal. This level can be permanently changed and stored in non-volatile memory.

Vout_UV_warn_limit (0x43)

Sets the value at which a warning will be issued that the output voltage is too low. The default UV_warning limit is set at $52V_{DC}$ (for - AT Version). Reduction below the warning value will set the Alert# signal. This level can be permanently changed and stored in non-volatile memory.

Vout_UV_fault_limit (0x44)

Sets the value at which the CC4500 will shut down if the output gets below this level when not in overload (see 0x48 for overload). The default UV_fault limit is set at $38V_{DC}$. This register is masked if the UV is caused by interruption of the input voltage to the CC4500. This level can be permanently changed and stored in non-volatile memory.

Vout_fault_response (0x45)

Sets the response if the output voltage falls below the UV_fault_limit. The default UV_fault_response is latched off (for - AT Version) (0x80). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

Iout_OC_fault_limit (0x46)

Sets the value at which the CC4500 will shut down at High Line. This level can be permanently changed and stored in non-volatile memory.

Iout_OC_fault_response (0x47)

Sets the response if the output overload exceeds the OC_Fault_limit value. The default OC_fault_response is latched (for - AT Version) (0xC0). The only two allowable states are latched (0xC0) or hiccup (0xF8). The default response state can be permanently changed and stored in non-volatile memory.

Iout_OC_LV_fault_limit (0x48)

Sets the value at which the CC4500 will shut down when the CC4500 is in overload and the output gets below this level. The default fault limit is set at $35V_{DC}$. This register is masked if the UV is caused by interruption of the input voltage to the CC4500. This level can be permanently changed and stored in non-volatile memory.

Iout_OC_warn_limit (0x4A)

Sets the value at which the CC4500 issues a warning that the output current is getting too close to the shutdown level at high line. This level can be permanently changed and stored in non-volatile memory.

OT_fault_limit (0x4F)

Sets the value at which the CC4500 responds to an OT event, sensed by the dc-sec sensor. The response is defined by the OT_fault_response register. Need to be lower than the internal value defined by the firmware to trigger the event.

OT_fault_response (0x50)

Sets the response if the output overtemperature exceeds the OT_Fault_limit value. The default OT_fault_response is hiccup (0xC0). The only two allowable states are latched (0x80) or hiccup. The default response state can be permanently changed and stored in non-volatile memory.

OT_warn_limit (0x51)

Sets the value at which the CC4500 issues a warning when the dc-sec temperature sensor exceeds the warn limit. Need to be lower than the internal value defined by the firmware to trigger the event.

Vin_OV_fault_limit (0x55)

Sets the value at which the CC4500 shuts down because the input voltage exceeds the allowable operational limit. The default Vin_OV_fault_limit is set at $300V_{AC}$.

Vin_OV_fault_response (0x56)

Sets the response if the input voltage level exceeds the Vin_OV_fault_limit value. The default Vin_OV_fault_response is latched off (0X80). (The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

Vin_OV_warn_limit (0x57)

This is a warning flag indicating that the input voltage is increasing dangerously close to the high input voltage shutdown level. The default Vin_OV_warn_limit is $295V_{AC}$ and by default should be set lower than Vin_OV_fault_limit

Vin_UV_warn_limit (0x58)

This is another warning flag indicating that the input voltage is decreasing dangerously close to the low input voltage shutdown level. The default UV_fault_limit is $170V_{AC}$.

Vin_UV_fault_limit (0x59)

Sets the value at which the CC4500 shuts down because the input voltage falls below the allowable operational limit. The default Vin_UV_fault_limit is set at $150V_{AC}$.

Vin_UV_fault_response (0x5A)

Sets the response if the input voltage level falls below the Vin_UV_fault_limit value. The default Vin_UV_fault_response is restart (0xC0).

STATUS_BYTE (0x78)

Returns one byte of information with a summary of the most critical device faults.

Bit	Flag	Default Value
7	Unit is busy	0
6	OUTPUT OFF	0
5	VOUT Overvoltage Fault	0
4	IOUT Overcurrent Fault	0
3	VIN Undervoltage Fault	0
2	Temperature Fault or	0
1	CML (Comm. Memory	0
0	None of the above	0

STATUS_WORD (0x79)

Returns status_byte as the low byte and the following high_byte.

Bit Position	Flag	Default Value
7	VOUT Fault or Warning	0
6	IOUT Fault or Warning	0
5	INPUT Fault or Warning	0
4	MFR SPECIFIC	0
3	POWER_GOOD# (is negated)	0
2	FAN Fault or Warning	0
1	OTHER	0
0	UNKNOWN Fault or Warning	0

STATUS_VOUT (0x7A)

Returns one byte of information of output voltage related faults.

Bit Position	Flag	Default Value
7	VOUT OV Fault	0
6	VOUT_OV_WARNING	0
5	VOUT_UV_WARNING	0
4	VOUT UV Fault	0
3 - 0	X	0

STATUS_IOUT (0x7B)

Returns one byte of information of output current related faults.

The OC Fault limit sets where current limit is set. The CC4500 actually shuts down below the LV fault limit setting.

Bit Position	Flag	Default Value
7	IOUT OC Fault	0
6	IOUT OC LV Fault	0
5	IOUT OC Warning	0
4	X	0
3	CURRENT SHARE Fault	0
2	IN POWER LIMITING MODE	0
1 - 0	X	0

STATUS_INPUT (0x7C)

Returns one byte of information of input voltage related faults.

Bit Position	Flag	Default Value
7	VIN_OV_Fault	0
6	VIN_OV_Warning	0
5	VIN_UV_ Warning	0
4	VIN_UV_Fault	0
3	Unit OFF for low input voltage	0
2	IIN_OC_Fault	0
1 - 0	X	0

STATUS_TEMPERATURE (0x7D)

Returns one byte of information of temperature related faults.

Bit Position	Flag	Default Value
7	OT Fault	0
6	OT Warning	0
5 - 0	X	0

STATUS_CML (0x7E)

Returns one byte of information of communication related faults.

Bit Position	Flag	Default Value
7	Invalid/Unsupported Command	0
6	Invalid/Unsupported Data	0
5	Packet Error Check Failed	0
4 - 2	X	0
1	Other Communication Fault	0
0	X	0

Read-back descriptions

Single parameter read backs

Functions can be read back one at a time using the read_word_protocol with PEC. A command is first sent out notifying the slave what function is to be read back followed by the data transfer.

Analog data is always transmitted LSB followed by MSB. A NA following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

Read back error

1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

1	8		1
Sr	Slave address	Rd	A

8	1	8	1	8	1	1
LSB	A	MSB	A	PEC	No-Ack	P

If the microcontroller does not have sufficient time to retrieve the requested data, it has the option to return all FF's instead of incorrect data.

Read_FRU (0x99, 0x9A, 0x9B, 0x9E)

Returns FRU information. Must be executed one register at a time.

1	8		1	8	1
S	Slave address	Wr	A	Command 0x9x	A

1	8		1	8	1
Sr	Slave address	Rd	A	Byte count = x	A

8	1	8	1	8	1	8	1	1
Byte_1	A	Byte	A	Byte_x	A	PEC	No-Ack	P

Mfr_ID (0x99)

Manufacturer in ASCII – 6 characters maximum, default is “ATOS” for CC4500AC55FB, otherwise OmniOn-PE to represent OmniOn Power Electronics.

Mfr_model (0x9A)

Manufacturer model-number in ASCII – 16 characters, for this unit: CC4500AC55FB (note the returned data will have sixteen characters, even if the normal product part number only has 14 or 15 characters, and that is why the remaining spaces are taken up with “x”.)

Mfr_revision (0x9B)

Total 8 bytes, this is the product series taking the form X:YZ. Each byte is in ASCII format. The series number is read from left to right, scanned from the series number bar code on the power supply. Unused characters are filled at the end with null

Mfr_serial (0x9E)

Product serial number includes the manufacturing date, manufacturing location in up to 16 characters. For example:

23CS06106902xxx, is decoded as:

23 – year of manufacture, 2023

CS – manufacturing location, in this case Shanghai, China

06 – week of manufacture

106902xxx – serial number, at manufacturers choice

Manufacturer-specific PMBus commands

Many of the manufacturer-specific commands read back more than two bytes. If more than two bytes of data are returned, the standard SMBus™ Block read

is utilized. In this process, the Master issues a Write command followed by the data transfer from the CC4500. The first byte of the Block Read data field sends back in hex format the number of data bytes, exclusive of the PEC number, that follows. Analog data is always transmitted LSB followed by MSB. A No-ack following the PEC byte signifies that the transmission is complete and is being terminated by the ‘host’.

Manufacturer_Specific Status and alarm registers

The content and partitioning of these registers is significantly different than the standard register set in the PMBus™ specification. More information is provided by these registers and they are either accessed rapidly, at once, using the ‘multi parameter’ read back scheme of this document, or in batches of two STATUS and two ALARM registers.

Status_summary (0xD0): This ‘manufacturer specific’ command is the basic read back returning STATUS and ALARM register data, output voltage, output current, and internal temperature data in a single read. Internal temperature should return the temperature that is closest to a shutdown level.

1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

1	8		1	8	1
Sr	Slave address	Rd	A	Byte count = 11	A

8	1	8	1	8	1	8	1
Status-2	A	Status-1	A	Alarm-3	A	Alarm-2	A

8	1	8	1	8	1
Alarm-1	A	Voltage LSB	A	Voltage MSB	A

8	1	8	1
Current LSB	A	Current MSB	A

8	1	8	1
Temp LSB	A	Temp MSB	A

8	1	1
PEC	No-Ack	P

Status_unit (0xD1)

This command returns the STATUS-2 and STATUS-1 register values using the standard 'read' format.

Status-2

Bit Position	Flag	Default Value
7	PEC Error	0
6	OC [hiccup=1,latch=0]	1
5	Invalid_Instruction	0
4	n/a	0
3	OR'ing Test Failed	0
2	n/a	0
1	Data_out_of_range	0
0	Remote ON/OFF [HI = 1]	x

Oring fault: Triggered either by the host driven or'ing test or by the repetitive testing of this feature within the CC4500. A destructive fault would cause an internal shutdown. Success of the host driven test depends on power capacity capability which needs to be determined by the external processor. Thus, a non-destructive or'ing fault does not trigger a shutdown.

Status-1

Bit Position	Flag	Default
7	OT [Hiccup=1, latch=0]	1
6	OR'ing_Test_OK	0
5	Internal_Fault	0
4	Shutdown	0
3	Service LED ON	0
2	External_Fault	0
1	LEDs_Test_ON	0
0	Output ON (ON = 1)	x

Status_alarm (0xD2)

This command returns the ALARM-3 - ALARM-1 register values.

Alarm-3

Bit Position	Flag	Default Value
7	Interlock open	0
6	Fuse fail	0
5	PFC-DC communications fault	0
4	DC-I²C communications fault	0
3	AC monitor communications fault	0
2	x	0
1	x	0
0	Or'ing fault	0

Alarm-2

Bit Position	Flag	Default Value
7	FAN_Fault	0
6	No_Primary	0
5	Primary_OT	0
4	DC/DC_OT	0
3	Vo lower than BUS	0
2	Thermal sensor filed	0
1	Stby_out_of_limits	0
0	Power_Delivery	0

Power Delivery: If the internal sourced current to the current share current is > 10A, a fault is issued.

Alarm-1

Bit Position	Flag	Default Value
7	POWER LIMIT	0
6	PRIMARY Fault	0
5	OT_Shutdown	0
4	OT_Warning	0
3	IN OVERCURRENT	0
2	OV_Shutdown	0
1	VOUT_out_of_limits	0
0	VIN_out_of_limits	0

Read input string (0xD4)

Reads back the input voltage and input power consumed by the CC4500.

1	7	1	1	8
S	Slave address	Wr	A	Command Code

1	1	7	1	1
A	Sr	Slave Address	Rd	A

8	1	8	1	8	1
Byte Count = 4	A	Voltage - LSB	A	Voltage - MSB	A

8	1	8	1	8	1	1
Power - LSB	A	Power - MSB	A	PEC	No-Ack	P

Read_firmware_rev (0xD5)

Reads back the firmware revision of all three microcontrollers in the CC4500.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	1	7	1	1	8	1
A	Sr	Slave Address	Rd	A	Byte Count = 6	A

8	1	8	1
Primary major rev	A	Primary minor rev	A

8	1	8	1
Secondary major rev	A	Secondary minor rev	A

8	1	8	1	8	1	1
I²C major rev	A	I²C revision	A	PEC	No-ack	P

Read_run_timer (0xD6)

This command reads back the recorded operational ON state of the CC4500 in hours. The operational ON state is accumulated from the time the CC4500 is initially programmed at the factory. The CC4500 is in the operational ON state both when in standby and when it delivers main output power. Recorded capacity is approximately 10 years of operational state.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	7	1	1	8	1
Sr	Slave Address	Rd	A	Byte count = 3	A

8	1	8	1	8	1
Time - LSB	A	Time	A	Time - MSB	A

8	1	1
PEC	No-ack	P

EEPROM record (0xD9)

The µC contains 128 bytes of reserved EEPROM space for customer use. After the command code, the starting memory location must be entered followed by a block write, and terminated by the PEC number:

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1
Start location	A	Byte count	A

8	1	.....	8	1
first_byte	A	.....	last - byte	A

8	1	1
PEC	A	P

To read contents from the EEPROM section

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1
Memory location	A	Byte count ≤ 32	A

1	7	1	1
Sr	Slave address	Rd	A

8	1	.....	8	1
Byte 1	A	.....	Byte ≤ 32	A

8	1	1
PEC	No-ack	P

Super Register 1 (0xDC)

This first clever 'super' register allows to read all in one those 8 registers to monitor the CC4500 and returning input power, input voltage, input current, output voltage, output current, internal temperatures for PFC, DC-PRI & DC SEC.

1	8	1	8	1
S	Slave address	Wr	A	Command Code	A

1	8	1	8	1
Sr	Slave address	Rd	A	Byte count = 17	A

8	1	8	1	8	1	8	1
PIN LSB	A	PIN MSB	A	VIN LSB	A	VIN MSB	A

8	1	8	1	8	1
IIN LSB	A	IIN MSB	A	VOUT LSB	A

8	1	8	1
VOUT MSB	A	IOUT LSB	A

8	1	8	1
IOUT MSB	A	TEMP_PFC LSB	A

8	1	8	1
TEMP_PFC MSB	A	TEMP_DC_PRI LSB	A

8	1	8	1
TEMP_DC_PRI MSB	A	TEMP_DC_SEC LSB	A

8	1	8	1	1
TEMP_DC_SEC MSB	A	PEC	No-Ack	P

Super Register 2 (0xDD)

This second clever 'super' register allows to read all in one those 6 registers to monitor the CC4500's status and returning Status of Word, VOUT, IOUT, INPUT, TEMPERATURE, CML.

1	8	1	8	1
S	Slave address	Wr	A	Command Code	A

1	8	1	8	1
Sr	Slave address	Rd	A	Byte count = 8	A

8	1	8	1	8	1	8	1
S_WORD	A	S_WORD	A	S_VOUT	A	S_IOUT	A

8	1	8	1	8	1
S_INPUT	A	S_TEMP	A	S_CML	A

8	1	1
PEC	No-Ack	P

Test Function (0xDF)

Bit	Function	State
7	25ms stretch for factory use	1= stretch ON
5 - 6	reserved	
4	Or'ing test	1=ON, 0=OFF
2 - 3	reserved	
1	Service LED	1=ON, 0=OFF
0	LED test	1=ON, 0=OFF

LEDs test ON

Will turn-ON simultaneously the front panel LEDs of the CC4500 sequentially 7 seconds ON and 2 seconds OFF until instructed to turn OFF. The intent of this function is to provide visual identification of the CC4500 being talked to and to visually verify that the LEDs operate and driven properly by the micro controller.

LEDs test OFF

Will turn-OFF simultaneously the four front panel LEDs of the CC4500.

Service LED ON

Requests the CC4500 to flash-ON the Service (ok-to-remove) LED. The flash sequence is approximately 0.5 seconds ON and 0.5 seconds OFF.

Service LED OFF

Requests the CC4500 to turn OFF the Service (ok-to-remove) LED.

OR'ing Test

This command verifies functioning of output OR'ing. At least two paralleled CC4500s are required. The host should verify that N+1 redundancy is established. If N+1 redundancy is not established the test can fail. Only one CC4500 should be tested at a time.

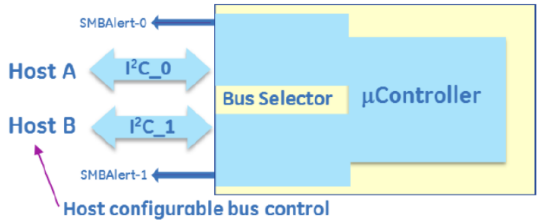
Verifying test completion should be delayed for approximately 30 seconds to allow the CC4500 sufficient time to properly execute the test.

Failure of the isolation test is not considered a CC4500 FAULT because the N+1 redundancy requirement cannot be verified. The user must determine whether a true isolation fault indeed exists.

Dual Master Control

Two independent I²C lines and Alert# signals provide true communications redundancy allowing two independent controllers to sequentially control the CC4500.

A short or an open connection in one of the I²C lines does not affect communications capability on the other I²C line. Failure of a 'master' controller does not affect the CC4500s and the second 'master' can take over control at any time when the bus is idle.



Conceptual representation of the dual I²C bus system

The Alert# line exciting the CC4500 combines the Alert# functions of CC4500 control and dual_bus_control.

Status_bus (0xD7)

Bus_Status is a single byte read back. The command can be executed by either master at any time independent of who has control.

The microcontroller may issue a clock stretch, as it can for any other instruction, if it requires a delay because it is busy with other activities.

Automatically resetting into the default state requires the removal of bias supply from the controllers.

Bit Position	Flag	Default Value
7	Bus 1 command error	0
6	Bus 1 Alert# enabled	0
5	Bus 1 requested control	0
4	Bus 1 has control of the PS	0
3	Bus 0 command error	0
2	Bus 0 Alert# enabled	0
1	Bus 0 requested control	0
0	Bus 0 has control of the PS	1

Command Execution

The master not in control can issue two commands on the bus, take_over_bus_control and clear_faults.

Take_over_bus_control (0xD8)

This command instructs the internal microcontroller to switch command control over to the 'master' that initiated the request. Actual transfer is controlled by the I²C selector section of the microcontroller. A bus transfer only occurs during an idle state when the 'master' currently in control (in the execution process of a control command) has released the bus by

issuing a STOP command. Control can be transferred at any time if the 'master' being released is executing a read instruction that does not affect the transfer of command control. Note: The microcontroller can handle read instructions from both busses simultaneously.

The command follows PMBus™ standards and it is not executed until the trailing PEC is validated.

Status Notifications

Once control is transferred both Alert# lines should get asserted by the I²C selector section of the microcontroller. The released 'master' is notified that a STATUS change occurred, and he is no longer in control. The connected 'master' is notified that he is in control and he can issue commands to the CC4500. Each master must issue a clear_faults command to clear his Alert# signal.

If the Alert# signal was triggered by the CC4500 and not the I²C selector section of the microcontroller, then only the 'master' in control can clear the CC4500 registers. Incomplete transmissions should not occur on either bus.

General Performance Descriptions

Default State

CC4500s are programmed in the default state to automatically restart after a shutdown has occurred. The default state can be reconfigured by changing non-volatile memory (Store_user_code).

Delayed overcurrent shutdown during startup

CC4500s are programmed to stay in a constant current state for up to 20 seconds during power up. This delay has been introduced to permit the orderly application of input power to a subset of paralleled CC4500s during power up. If the overload persists beyond the 20 second delay, the CC4500 will revert to its programmed state of overload protection.

Unit in Power Limit or in Current Limit

When output voltage is > 40V_{DC} the Output LED will continue blinking. When output voltage is < 40V_{DC}, if the unit is in the RESTART mode, it goes into hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output LED is OFF. When the unit is in latched shutdown the output LED is OFF.

Restart after a latchoff

PMBus™ fault_response commands can be configured to direct the CC4500 to remain latched off for over_voltage, over_temperature and over_current.

To restart after a latch off either of five restart mechanisms are available.

1. The hardware pin ON/OFF may be cycled OFF and then ON.
2. The unit may be commanded to restart via I²C through the Operation command by cycling the output OFF followed by ON.
3. Remove and reinsert the unit.
4. Turn OFF and then turn ON AC power to the unit.
5. Changing firmware from latch off to restart.

Each of these commands must keep the CC4500 in the OFF state for at least 2 seconds, with the exception of changing to restart. A successful restart shall clear all alarm registers, set the restarted successful bit of the Status_2 register.

A power system that is comprised of a number of CC4500s could have difficulty restarting after a shutdown event because of the non-synchronized behaviour of the individual CC4500s. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by:

1. Issuing a GLOBAL OFF and then ON command to all CC4500s,
2. Toggling Off and then ON the ON/OFF (ENABLE) signal
3. Removing and reapplying input commercial power to the entire system.

The CC4500s should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual CC4500s.

Auto_restart

Auto-restart is the default configuration for over-current and over-temperature shutdowns. These features are configured by the PMBus™ fault_response commands.

An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again.

Fault Management

The CC4500 recognizes that certain transitionary states can occur before a final state is reached. The STATUS and ALARM registers will not be frozen into a notification state until the final state is reached. Once a final state is reached the Alert# signal is set and the STATUS and ALARM registers will not get reinstated until a clear_faults is issued by the master. The only exception is that additional state changes may be added to the original list if further changes are noted.

The CC4500 differentiates between internal faults that are within the CC4500 and external faults that the CC4500 protects itself from, such as overload or input voltage out of limits. The FAULT LED, FAULT PIN or i^2C alarm is not asserted for EXTERNAL FAULTS. Every attempt is made to annunciate External Faults. Some of these annunciations can be observed by looking at the input LEDs. These fault categorizations are predictive in nature and therefore there is a likelihood that a categorization may not have been made correctly.

Input voltage out of range

The Input LED will continue blinking as long as sufficient power is available to power the LED. If the input voltage is completely gone the Input LED is OFF.

State Change Definition

A state_change is an indication that an event has occurred that the MASTER should be aware of. The following events shall trigger a state_change:

- Initial power-up of the system when AC gets turned ON. This is the indication from the CC4500 that it has been turned ON. Note that the master needs to read the status of each CC4500 to reset the system_interrupt.
- Any changes in the bit pattern of either the PMBus standard STATUS or the mfr_specific STATUS registers should trigger the Alert# signal.

Smart Hot plug

The wide output capability of this CC4500 requires special controls when the CC4500 gets plugged into a live backplane.

During hot plug the CC4500 attempts to configure itself into the bus voltage setting of a working system. When inserted into the system the output of the CC4500 will be off.

- Prior to turning ON the main output, the CC4500 reads the voltage present on the bus. If the bus voltage is ≥40V the CC4500 will check whether Vmargin and the bus voltage are in agreement with each other.
- If there is agreement between Vmargin and the bus voltage, the CC4500 will proceed to turn ON its output utilizing the delayed overcurrent shutdown during turn-ON.
- If there is no agreement between Vmargin and the bus voltage, the CC4500 recognizes that the bus voltage is being controlled externally. In this case the CC4500 will keep its output OFF and will wait for the controller based output voltage command. Once such a command is received from the controller, the CC4500 will proceed with normal turn-ON utilizing the delayed overcurrent shutdown.
- The CC4500 continues to monitor Vmargin and the bus voltage. If no command is received from the controller, and if Vmargin and the bus voltage should agree at a later time, then the CC4500 will normally turn ON it output utilizing the delayed overcurrent shutdown.
- If the bus voltage is <40V, the CC4500 proceeds with normal turn-ON into either its default voltage level or the voltage level commanded externally by Vmargin.

Failure Predictions

Alarm warnings that do not cause a shutdown are indicators of potential future failures of the CC4500. For example, if a thermal sensor failed, a warning is issued but an immediate shutdown of the CC4500 is not warranted. The goal is to identify problems early before a protective shutdown would occur that would take the CC4500 out of service.

Information only alarms

The following alarms are for information only, they do not cause a shutdown

- Over temperature warning
- Main output voltage out-of-limits
- Output voltage lower than bus
- Unit in Power Limit
- Thermal sensor failed
- Or'ing (Isolation) test failure
- Power delivery
- Stand-by output out of limits
- Communication errors

Remote Upgrade

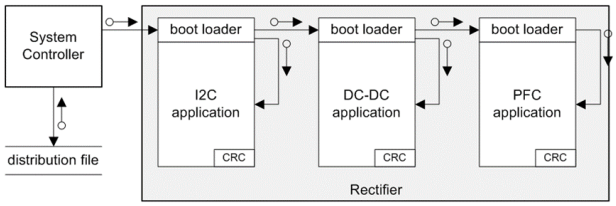
This section describes at a high-level the recommended re-programming process for the three internal microcontrollers inside the CC4500 when the re-programming is implemented in live, running, systems.

The process has been implemented in visual basic by OmniOn for controller-based systems positioned primarily for the telecommunications industry. OmniOn will share its development with customers who are interested to deploy the re-programming capability into their own controllers.

For some customers, internal system re-programming is either not feasible or not desired. These customers may obtain a re-programming kit from OmniOn. This kit contains a turn-key package with the re-program firmware.

Concept Description

The CC4500 contains three independent microcontrollers. The boost (PFC) section is controlled by the primary microcontroller. The secondary DC-DC converter is controlled by the secondary microcontroller, and I^2C communications are handled by the I^2C Interface microcontroller.



Each of the microcontrollers contains a boot loader section and an application section in memory. The purpose of the boot loader section is to facilitate the upgrading capability described here. All the commands for upgrading and memory space required for incrementally changing the application code are in this section. The application section contains the running code of the CC4500.

The system controller receives the upgrade package. It should first check whether an upgrade is required followed by upgrading those processors, one at a time, that are required to be upgraded. Each processor upgrade needs to be validated and once the upgrade is successfully completed the boot loader within each processor will permit the application to run after a reset. If the validation fails the boot loader will stay in its section. The system controller can attempt another upgrade session to see if it would complete successfully.

The upgrade package

This package contains the following files:

- Manifest.txt - The manifest describes the contents of the upgrade package and any incidental information that may be useful, for example, what this upgrade contains or why is this upgrade necessary. This file contains the version number and the compatibility code of the upgraded program for each of the three processors.

- Program.bin - The upgraded program contents are located here. Each processor to be upgraded will have its own file.

Below is an example of an upgrade package

- Contents of the upgrade are in a zip file CC4500AC55FBAT.zip
- Unzipping the contents shows the following files CC4500AC55FBAT_PFC.bin CC4500AC55FBAT_SEC.bin manifest.txt
- Opening manifest.txt shows the following # Upgrade manifest file # Targets: CC4500AC55FBAT PFC and SEC # Date: # Notes:
- Program contents

>p, CC4500AC55FBAT_P01, CC4500AC55FBAT _PFC.bin,1.x

>s,CC4500AC55FBAT_S01,CC4500AC55FBAT_SEC.bin,1.x

>i, CC4500AC55FBAT_I01, CC4500AC55FBAT_IIC.bin,1.x

compatibility code, new program, revision number

Upgrade Status Indication

The FAULT LED is utilized for indicating the status of the re-programming process.

Status	Fault LED	Description
Idle	OFF	Normal state
In boot block	Wink	Application is good
Upgrading	Fast blink	Application is erased or
Fault	ON	Erase or re-program failed

Wink: 0.25 seconds ON, 0.75 seconds OFF

Fast Blink: 0.25 seconds ON. 0.25 seconds OFF

Upgrade Procedure

1. Initialization: To execute the re-programming/ upgrade in the system, the CC4500 to be re-programmed must first be taken OFF-line prior to executing the upgrade. If the CC4500 is not taken OFF-line by the system controller, the boot loader will turn OFF the output prior to continuing with the re-programming operation. Note: Make sure that sufficient power is provided by the remaining on-line CC4500s so that system functionality is not jeopardized.
2. Unzip the distribution file
3. Unlock upgrade execution protection by issuing the command below:

Password(0xE0): This command unlocks the upgrade commands feature of the CC4500 by sending the characters 'UPGD'. (optional)

1	8		1	8	1	8	1
S	Slave	Wr	A	Command	A	Byte count = 4	A

8	1		8	1	8	1	1
Byte 0 - U	A	....	Byte 4 - D	A	PEC	A	P

4. Obtain a list of upgradable processors (optional)

Target list(0xE1): This command returns the upgradable processors within the CC4500. The byte word is the ASCII character of the processor (p, s, and i). The command is optional to the user for information only.

1	8		1	8	1
S	Slave address	Wr	A	Command code	A

1	8		1	8	1
Sr	Slave address	Rd	A	Byte count = 4	A

8	1	.....	8	1	8	1	1
Byte 0	A		Byte n	A	PEC	No-Ack	P

Potential target processors are the following:

p – primary (PFC)

s – secondary (DC-DC)

i – I^2C

5. Verify upgrade compatibility by matching the upgrade compatibility code in the manifest.txt file to the CC4500 compatibility code of the target processor.

Compatibility code (0xE2): This read command consists of up to 32 characters defining the hardware configuration:

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Command	A	Target-x	A

1	8		1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count = 32	A	Byte 0	A

	8	1	8	1	1
.....	Byte 31	A	PEC	No-Ack	P

Where Target-x is an ASCII character pointing to the processor to be updated:

p – primary (PFC)

s – secondary (DC-DC)

i – I^2C

6. Check the software revision number of the target processor in the CC4500 and compare it to the revision in the upgrade. If the revision numbers are the same, or the CC4500 has a higher revision number then no upgrade is required for the target processor.

Software revision(0xE3): This command returns the software revision of the target.

1	8		1	8	1	8	1
S	Slave	Wr	A	Command	A	Target-x	A

1	8		1	8	1	8	1
Sr	Slave	Rd	A	Byte count = 7	A	Major	A

8	1	8	1	8	1	8	1
Minor revision	A	month	A	day	A	year[16]	A

8	1	8	1	8	1	1
hrs	A	min	A	PEC	No-Ack	P

7. Verify the capability of each processor

Memory capability (0xE4): Provides the specifics of the capability of the device to be reprogrammed

1	8		1	8	1	8	1
S	Slave	Wr	A	Command	A	Target-x	A

1	8		1	8	1	8	1
Sr	Slave	Rd	A	Byte count =	A	Max	A

8	1	8	1	8	1	8	1
ET - LSB	A	ET - MSB	A	BT - LSB	A	BT - MSB	A

8	1	8	1	8	1	1
App_CRC - LSB	A	App_CRC - MSB	A	PEC	No-Ack	P

[16]Last two digits

Where the field definitions are shown as below:

Max Bytes	Maximum number of bytes in a data packet
ET	Erase time for entire application space (in mS)
BT	Data packet write execution time (uS)
APP_ CRC	Application CRC-16 – returns the application CRC-16 calculation. Reading these register values, if the application upload CRC-16 calculation returns an invalid, provides the mismatch information to the host program. (See application status(0xE5) command)

This information should be used by the host processor to determine the maximum data packet size and add appropriate delays between commands.

8. Verify availability: The Application status command is used to verify the present state of the boot loader.

Application status (0xE5): Returns the Boot Loader's present status

1	8		1	8	1	8	1
S	Slave	Wr	A	Command	A	Target-x	A

1	8		1	8	1	8	1	1
Sr	Slave	Rd	A	Status	A	PEC	No-	P

Status bits:

Status of the application should be checked after the execution of successive commands to verify that the commands have been properly executed.

0x00	Processor is available	0x10	Reserved
0x01	Application erased	0x20	Reserved
0x02	CRC-16 invalid	0x40	Manages downstream µC
0x04	Sequence out of order	0x80	In boot loader
0x08	Address out of range		

9. Issue a Boot Loader command with the enter boot block instruction

Boot loader (0xE6): This command manages the upgrade process starting with entering the sector, erasing the present application, indicating completion of the upload and finally exiting from the boot sector, thereby turning over control to the uploaded application.

1	7	7	7	8	1	8	1
S	Slave address	Wr	A	Command code	A	Target-x	A

8	1	8	1	1
Data	A	PEC	A	P

Data:

1 = enter boot block (software reboot)

2 = erase

3 = done

4 = exit[17] boot block (watchdog reboot)

Note: The target microcontroller field is ignored for enter and exit commands. During this process if the output of the CC4500 was not turned OFF the boot loader will turn OFF the output

10. Erase and program each microcontroller using the Boot Loader command, starting with the PFC.

11. Wait at least 1 second after issuing an erase command to allow the microcontroller to complete its task.

12. Use command 0xE5 to verify that the PFC microcontroller is erased. The returned status byte should be 0x81.

13. Use the Data Transfer command to update the application of the target microcontroller.

Data transfer (0xE7): The process starts with uploading data packets with the first sequence number (0x0000).

[17]The 'exit boot block' command is only successful if all applications are valid, otherwise, control remains in the boot block

1	8		1	8	1	8	1
S	Slave	Wr	A	Command	A	Target-x	A

8	1	8	1	8	1
Seq-LSB	A	Seq-MSB	A	Byte Count ≤32	A

8	1		8	1	8	1	1
Byte 0	A	.....	Byte n-1	A	PEC	A	P

After completion of the first data packet upload the Boot loader increments the sequence number. A subsequent read to the boot loader will return the incremented sequence number and a STATUS byte. This is a validity check to ensure that the sequence number is properly kept. The returned STATUS byte is the same as the application status response. It is appended here automatically to save the execution of another command. It should be checked to ensure that no errors are flagged by the boot loader during the download. If an error occurred, terminate the download load and attempt to reprogram again.

1	8		1	8	1
S	Slave address	Wr	A	Command code	A

1	8		1	8	1
Sr	Slave address	Rd	A	Byte count ≤32	A

1	8	8	1	8	1	8	1	1
Seq-LSB	A	Seq-MSB	A	Status	A	PEC	No-Ack	P

Sequence number validation takes place after each data block transfer. The next data block transfer starts with the sequence number received from the boot loader.

The host keeps track of the upload and knows when the upload is completed.

14. Execute a Boot loader command to tell the PFC microcontroller that the transfer is done. At the completion signal, the PFC microcontroller should calculate the PEC value of the entire application. The last two bytes of the loaded application were the CRC-16 based PEC calculation. Wait for at least 1 second to allow time for the PFC microcontroller to calculate the error checking value.

15. Execute an Application status command to verify that the error check is valid. The returned status should be 0x80.
16. Execute a Boot loader command to exit boot block. Upon receipt of the command the PFC microcontroller will transfer to the uploaded application code.
17. Wait for at least 1 second.
18. Use command 0xE1 to verify that the PFC microcontroller is now in the application code. The returned status data byte should be 0x00.
19. Repeat the program upgrade for the Secondary and I²C microcontrollers, if included in the upgrade package.

Product Comcode

Although the comcode number is not required for the upgrade process in its present form, it may be useful when upgrading multiple version of the same product in order to differentiate product upgrade requirements.

1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

1	8		1	8	1
Sr	Slave address	Rd	A	Byte count = 11	A

8	1		8	1	8	1	1
Byte 0	A	.....	Byte 10	A	PEC	No-Ack	P

Error Handling

The Boot loader will not start the application if errors occurred during the re-program stage. The controlling program could restart the upgrade process or terminate the upgrade and remove the offending CC4500 from service.

Black Box

Contents of the black box and more detailed information about the specifics of the feature are described in a separate document. The intent here is to provide a high-level summary This feature includes the following:

1. A rolling event Recorder

2. Operational Use Statistics

The Rolling Event Recorder

The purpose of the black box is to provide operational statistics as well as fault retention for diagnostics following either recoverable or non-recoverable fault events. Sufficient memory exists to store up to 5 time-stamped snapshot records (pages) that include the state of the status and alarm registers and numerous internal measurement points within the CC4500. Each record is stored into non-volatile memory at the time when a black box trigger event occurs. Once five records are stored, additional records over-write the oldest record.

The memory locations will be cleared, when the product is shipped from the OmniOn factory.

Operational Use Statistics

This feature of the black box includes information on the repetition and duration of certain events in order to understand the long-term operational state of the CC4500. The events are placed into defined buckets for further analysis. For example: the CC4500 records how long was the output current provided in certain load ranges.

Accessing the event records

The event records are accessed by uploading the entire contents of the black box of the CC4500 into a folder assigned by the user. Within the I²C protocol this upload is accomplished by the upload_black_box (0xF0) command described below. OmniOn provides a Graphical User Interface (GUI) that de-codes the contents of the black box into a set of records that can be reviewed by the user.

Upload Black box (0xF0)

This command executes the upload from the CC4500 to a file of the user's choice.

The 100ms delay prior to the restart is mandatory to provide enough time for the CC4500 to gather the required data from the secondary DSP controller.

1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1
Start address - MSB	A	Start address - LSB	A

8	1
Length = N (≤ 32)	A

..... delay

1	8		1	8	1	8	1
Sr	Slave	Rd	A	Length ≤ 32	A	Byte 0	A

...	8	1	8	1	1
	Byte N-1	A	PEC	No-Ack	P

If a transmission error occurs, or if the microcontroller did not receive the data from the DSP, the microcontroller may set the length to 0, issue a PEC and terminate the transmission.

The data array supported by the OmniOn Interface Adapter is 32 x 64 comprising 2048 bytes of data.

Start Address	0 ..... Byte 31
0000h	
0020h	
0040h	
.	
.	
.	
.	
.	
.	
07E0h	

PMBus Command Summary (besides special ones)

Command	Hex Code	Data Field	Non-Volatile Memory Storage[18] / Default
Operation	0x01	1	Yes/80
Clear_Faults	0x03	-	
Write _Protect	0x10	1	Yes/00
Restore_default_all	0x12	-	
Restore_user_all	0x16	-	
Store_user_code	0x17	1	Yes
Restore_user_code	0x18	1	
Vout_mode	0x20	1	
Vout_command	0x21	2	Yes / 55
Vin_ON	0x35	2	
Vin_OFF	0x36	2	
Vout_OV_fault_limit	0x40	2	Yes / 60
Vout_OV_fault_response	0x41	1	No / 80
Vout_OV_warn_limit	0x42	2	Yes / 59
Vout_UV_warn_limit	0x43	2	Yes / 52
Vout_UV_fault_limit	0x44	2	Yes /40
Vout_UV_fault_response	0x45	1	No / C0
Iout_OC_fault_limit	0x46	2	Yes / 83
Iout_OC_fault_response[19]	0x47	1	Yes / F8
Iout_OC_LV_fault_limit	0x48	2	Yes/35
Iout_OC_warn_limit	0x4A	2	Yes / 82
OT_fault_limit	0x4F	2	Yes/ 100
OT_fault_response[20]	0x50	1	Yes / C0
OT_warn_limit	0x51	2	Yes/95
Vin_OV_fault_limit	0x55	2	No/ 300
Vin_OV_fault_response	0x56	1	No/ C0
Vin_OV_warn_limit	0x57	2	Yes / 295
Vin_UV_warn_limit[21]	0x58	2	Yes / 170
Vin_UV_fault_limit[22]	0x59	2	No / 165
Vin_UV_fault_response	0x5A	1	No/ C0
Status_byte	0x78	1	
Status_word (+ byte)	0x79	1	
Status_Vout	0x7A	1	
Status_Iout	0x7B	1	
Status_Input	0x7C	1	
Status_temperature	0x7D	1	
Status_CML	0x7E	1	
Read_Vin	0x88	2	
Read_Iin	0x89	2	
Read_Vout	0x8B	2	
Read_Iout	0x8C	2	
Read_temp_PFC	0x8D	2	
Read_temp_dc_pri	0x8E	2	
Read_temp_dc_sec	0x8F	2	
Read_Pin	0x97	2	
Mfr_ID	0x99	6	
Mfr_model	0x9A	16	
Mfr_revision	0x9B	8	
Mfr_serial	0x9E	16	
Status_summary	0xD0	11	
Status_unit	0xD1	2	
Status_alarm	0xD2	3	
Read_input	0xD4	5	
Read_firmware_rev	0xD5	6	
Read_run_timer	0xD6	3	
Status_bus	0xD7	1	
Take_over_bus_control	0xD8		
EEPROM Record	0xD9	128	Yes
Super Register 1	0xDC	17	
Super Register 2	0xDD	8	
Reserved for factory use	0xDE		
Test_Function	0xDF	1	

PMBus Command Summary (besides special ones) (continued)

Command	Hex Code	Data Field	Non-Volatile Memory Storage/Default
Upgrade commands			
Password	0xE0	4	
Target_list	0xE1	4	
Compatibility_code	0xE2	32	
Software_version	0xE3	7	
Memory_capability	0xE4	7	
Application_status	0xE5	1	
Boot_loader	0xE6	1	
Data_transfer	0xE7	≤32	
Product comcode	0xE8	11	
Upload_black_box	0xF0	≤32	

[18]Yes – indicates that the data can be changed by the user

[19]Only latched (0xC0) or hiccup (0xF8) are supported

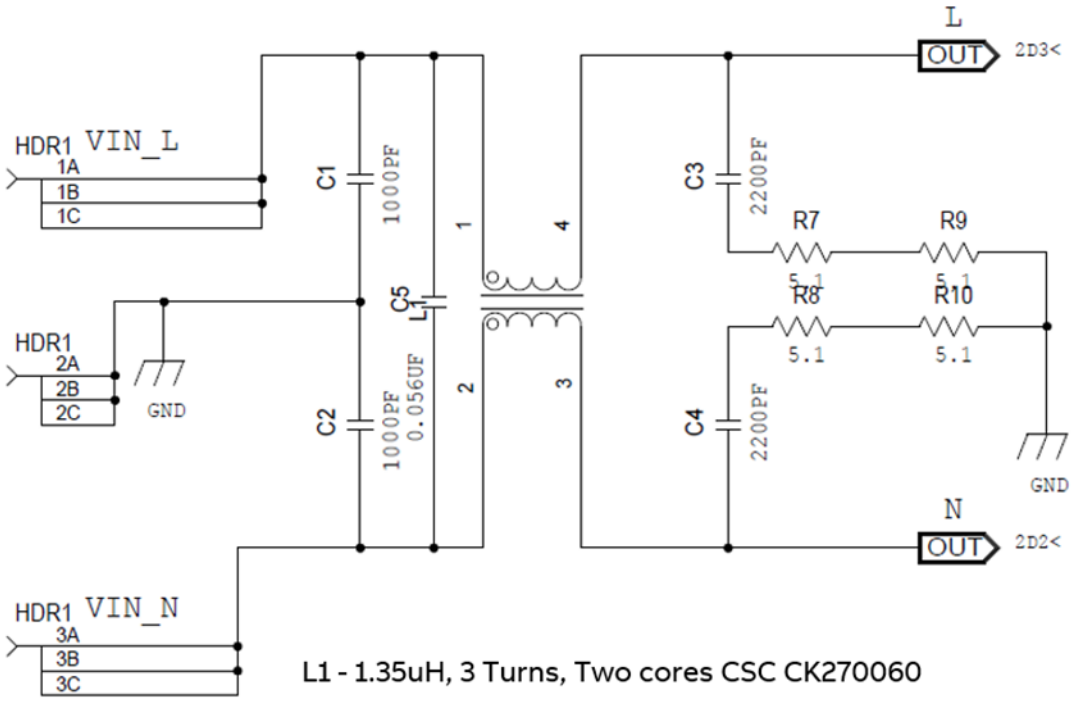
[20]Only latched (0x80) or restart (0xC0) are supported

[21]Recovery set at 90V

[22]Recovery set at 86V

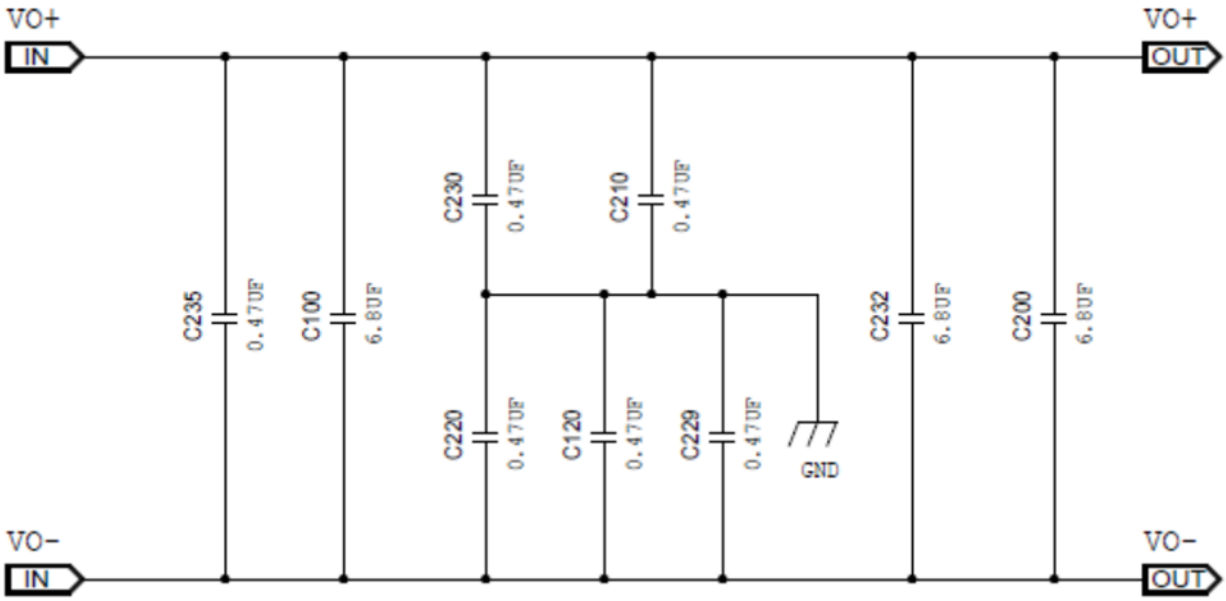
External EMI filter reference design

Input EMI filter circuit:



L1 - 1.35uH, 3 Turns, Two cores CSC CK270060

Output EMI filter circuit:



Alarm and LED state summary

	Rectifier LED State					Monitoring Signals			
Condition	AC OK Green	DC OK Green	Service Amber	Fault Red		Fault	OTW	PG	Module Present
OK	1	1	0	0		HI	HI	HI	LO
Thermal Alarm (5C before shutdown)	1	1	1	0		HI	LO	HI	LO
Thermal Shutdown	1	0	1	1		LO	LO	LO	LO
Blown AC Fuse in Unit	1	0	0	1		LO	HI	LO	LO
AC Present but not within limits	Blinks	0	0	0		HI	HI	LO	LO
AC not present[1]	0	0	0	0		HI	HI	LO	LO
Boost Stage Failure	1	0	0	1		LO	HI	LO	LO
Over Voltage Latched Shutdown	1	0	0	1		LO	HI	LO	LO
Over Current	1	Blinks	0	0		HI	HI	Pulsing[4]	LO
Non-catastrophic Internal Failure[2]	1	1	0	1		LO	HI	HI	LO
Standby (remote)	1	0	0	0		HI	HI	LO	LO
Service Request (PMBus mode)	1	1	Blinks	0		HI	HI	HI	LO
Communications Fault (RS485 mode)	1	1	0	Blinks		HI	HI	HI	LO

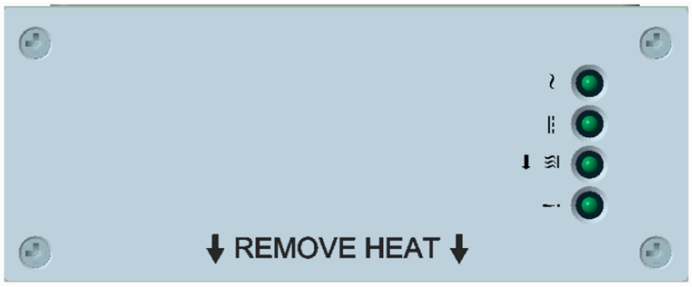
[1]This signal is correct if the rectifier is back biased from other rectifiers in the shelf .
[2]Any detectable fault condition that does not cause a shutting down. For example, ORing FET failure, boost section out of regulation, etc.
[3]Signal transition from HI to LO is output load dependent
[4]Pulsing at a duty cycle of 1ms as long as the unit is in overload.

Signal Definitions

All hardware alarm signals (Fault#, PG#, OTW#) are open drain FETs. These signals need to be pulled HI to either 3.3V or 5V. Maximum sink current 5mA. An active LO signal (< 0.4V_{DC}) state. All signals are referenced to LOGIC_GND unless otherwise stated.
Add PG#(A4) Power Fail Warning - Active low, open drain, 5V tolerant.

Function	Label	Type	Description
Output control	ON/OFF	Input	If shorted to Logic_GND main output is ON in Analog or PMBus mode.
Power Good Warning	PG#	Output	Open drain FET; Changes to LO if an imminent loss of the main output may occur
I²C Interrupt	Alert#_0/Alert#_1	Output	This signal is pulled to 3.3V via a 10kΩ resistor. Active LO
Rectifier Fault	Fault#	Output	An open drain FET; normally HI, changes to LO
Module Present	MOD_PRES	Output	Short pin, see Status and Control description for further information on this signal
Interlock	Interlock	Input	Short pin, controls main output during hot-insertion and extraction. Ref: Vout (-)
Protocol select	Protocol	Input	Selects operational mode. Ref: Vout (-). No-connect PMBus, 10kΩ - RS485
Margining	Vprog	Input	Changes the set point of the main output
Over-Temperature Warning	OTW#	Output	Open drain FET; normally HI, changes to LO 5°C prior to thermal shutdown
I²C address	Unit_ID	Input	Voltage level selecting the A3 - A0 bits of the address byte
I²C address	Rack_ID	Input	Voltage level selecting the A3 – A0 bits of the address byte
Back bias	8V_INT	Bi-direct	Used to back bias the DSP from operating Rectifiers. Ref: Vout (-)
Standby power	5VA	Output	5V at 2A provided for external use
Current Share	Ishare	Bi-direct	A single wire active-current-share interconnect between rectifiers Ref: Vout (-)
I²C Line 0	SCL_0	Input	PMBus line 0
I²C Line 0	SDA_0	Bi-direct	PMBus line 0
I²C Line 1	SCL_1	Input	PMBus line 1.
I²C Line 1	SDA_1	Bi-direct	PMBus line 1.
RS485 Line	RS_485+	Bi-direct	RS485 line +
RS485 Line	RS_485-	Bi-direct	RS485 line -

Front Panel LEDs



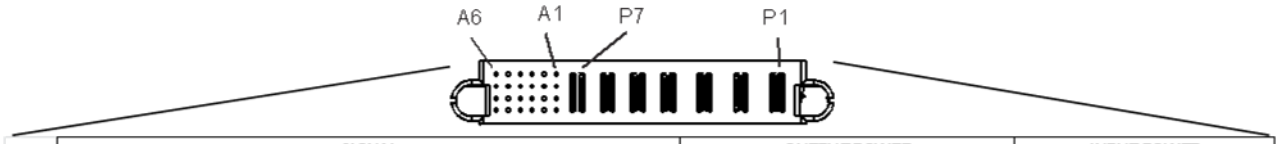
	Analog Mode	I²C Mode	RS485 Mode
~	←	**ON:** Input ok **Blinking:** Input out of limits	→
Heat	←	**ON:** Output ok **Blinking:** Overload	→
⎓	**ON:** Over - Temperature Warning	**ON:** Over - Temperature Warning **Blinking:** Overload	**ON:** Over - Temperature Warning
!	←	**ON:** Fault	→	**ON:** Fault **Blinking:** loss of communications

Output Connecter TE: 3-6450832-8, or FCI: 10106262-7006001LF

Mating Connector:

right angle PWB mate – all pins: TE – 1-6450872-6, FCI – 10106264-7006001LF;

right angle PWB mate except pass-thru input power: TE – 6450874-3, FCI – 10106265- 70CB001LF



	SIGNAL						OUTPUT POWER				INPUT POWER		
	6	5	4	3	2	1	P7	P6	P5	P4	P3	P2	P1
A	SCL_0	MOD_PRES	PG#	LOGIC_GND	RS_485+	Slot_ID							
B	SCL_1	OTW#	Alert#_0	Alert#_1	RS_485-	8V_INT	V_OUT	V_OUT	V_OUT	V_OUT	EARTH	LINE-2	LINE-1
C	SDA_0	Vprog	ON/OFF	Rack_ID	Ishare	Protocol	(-)	(+)	(+)	(-)	(GND)	(Neutral)	(HOT)
D	SDA_1	Fault#	5VA	Unit_ID	Interlock	Shelf_ID							

Note: Connector is viewed from the rear positioned inside the rectifier
Signal pins columns 1 and 2 are referenced to V_OUT (–). Slot_ID and Shelf_ID are used only with RS485 communications.
Signal pins columns 3 through 6 are referenced to Logic GND
Last to make-first to break shortest pin
Earth — First make-last to break longest pin implemented in the mating connector

Bus Transfer Reporting

This is as per CC4500 bus transfer reporting.

The events below concentrate on what happens when a clear_faults is issued. The system controller needs to be intelligent enough to inquire the status of the power supply before issuing a clar_faults. Otherwise, it would lose whatever information may be in the status registers.

	operation	Alert#1	Alert#0	status_bus	status_word	status_cml	
1	i2c1-command sent, not in control	1	0	0xC1	0x0000	0x00	
2	i2c1 issues a clear_faults	0	0	0x01	0x0000	0x00	
3	i2c0 in control, unit issues a fault	1	1	0x01	event1	0x00	
4	i2c1 takes over control	1	1	0x74	event1	0x00	
5	i2c1 read system status	1	1	0x74	event1	0x00	controller needs to read status before clearing the registers.
6	i2c1 issues a clear_faults	0	1	0x14	0x0000	0x00	Assuming that the event has cleared
7	i2c0 reads system status	0	1	0x14	0x0000	0x00	the Alert remains because of status_bus, not because of unit fault
8	i2c0 issues clear faults	0	0	0x10	0x0000	0x00	
9	i2c0 in control, unit issues a fault	1	1	0x01	event1	0x00	
10	i2c0 issues clear faults	0	0	0x01	0x0000	0x00	Assuming that the event has cleared
11	i2c1 in control	0	0	0x10	0x0000	0x00	
12	i2c0 takes over control	1	1	0x47	0x0000	0x00	
13	i2c0 issues a clear_faults	1	0	0x41	0x0000	0x00	
14	i2c1 issues a clear_faults	0	0	0x01	0x0000	0x00	
15	i2c1 in control	0	0	0x10	0x0000	0x00	
16	i2c0 issues a command	0	1	0x1C	0x0000	0x00	the command is rejected because i2c0 is not in control
17	i2c0 issues a clear_faults	0	0	0x10	0x0000	0x00	
18	i2c1 issues a bad command	1	0	0x10	0x0002	0x80	
19	i2c1 issues a clear_faults	0	0	0x10	0x0000	0x00	

Rules:
Side in control is the only one that can clear the Status registers.
The side in control cannot clear the alert of the side not in control
A power supply alarm should not set the status_bus registers

Mechanical Outline & Mounting screw positions

Outer dimensions (excluding protruding connector):

365 x 105 x 46mm (14.37 x 4.13 x 1.81 in)

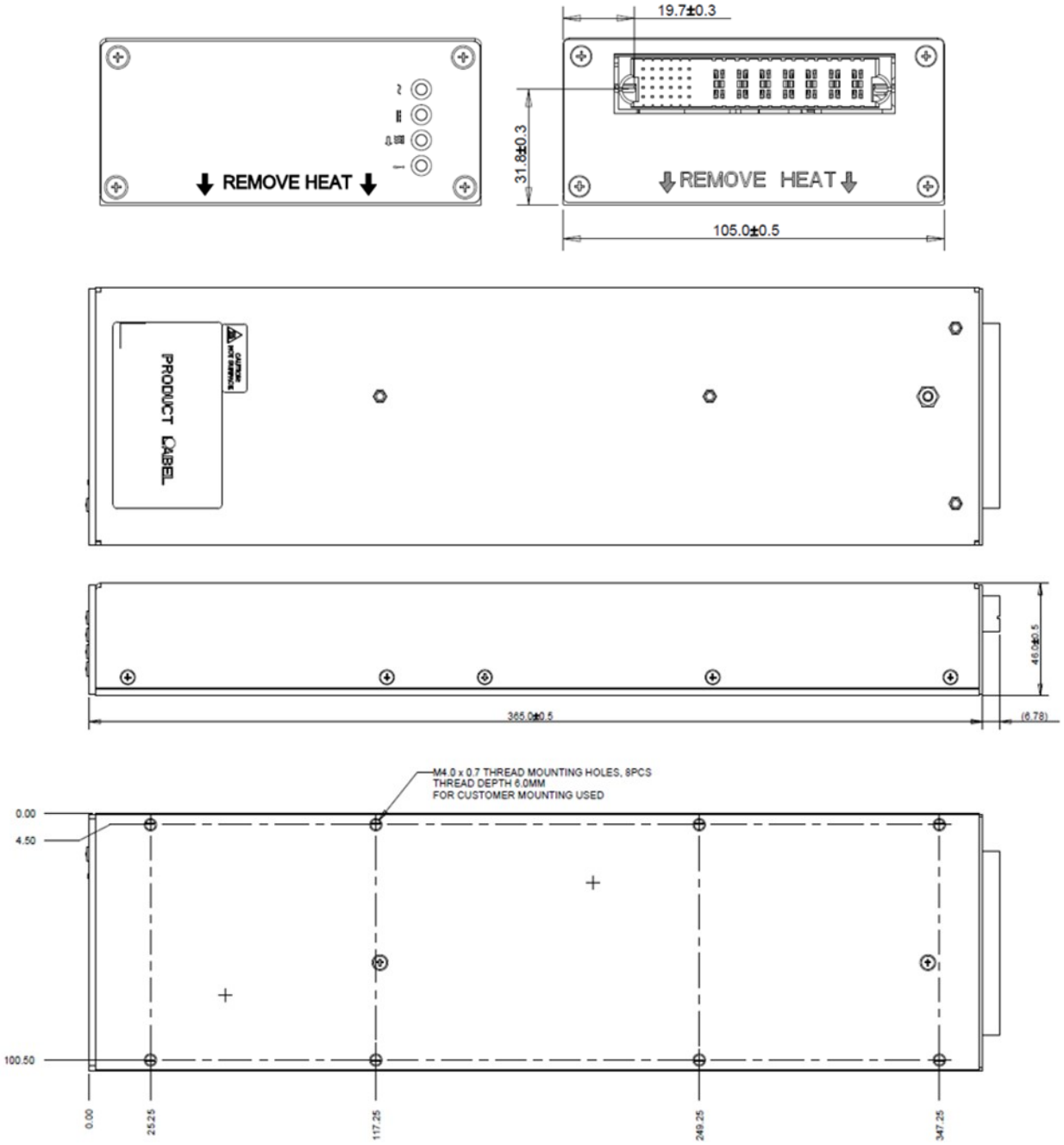
Unless otherwise specified all dimensions are in mm, non-limited

dimensions, other than size of raw

Material shall be held as follows when expressed:

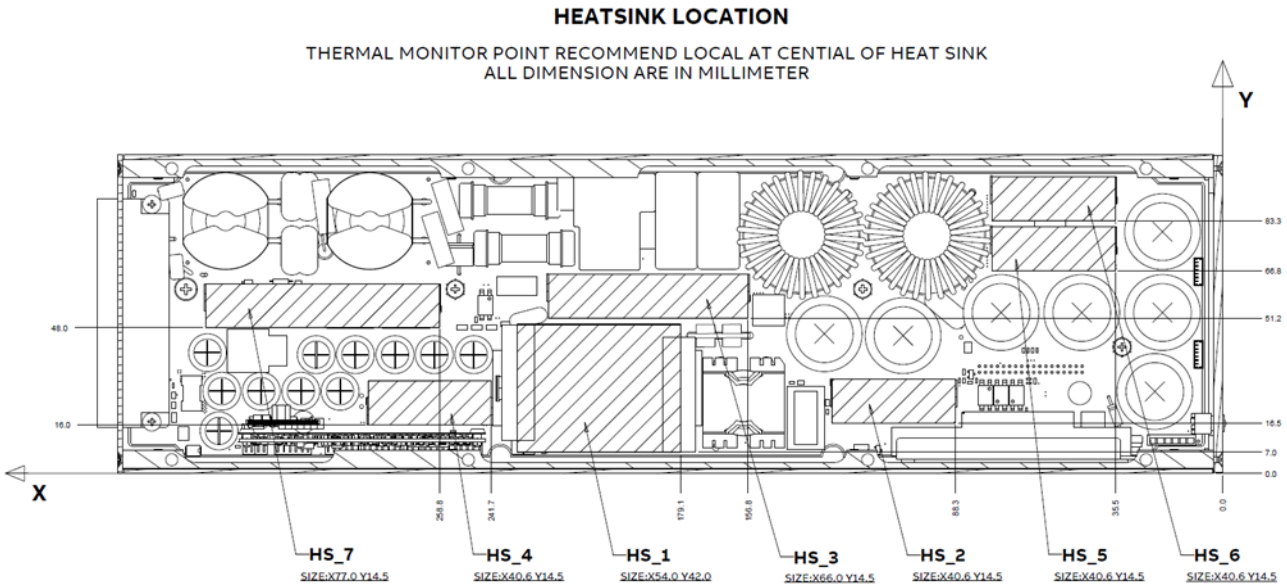
To no decimal places 0.5

To 1 and 2 decimal places 0.2



Temperature Monitoring Location

The following graphic shows the heatsink location, and heatsinks are the hot spots, should maintain the surface temperature above these hot spots at the recommended operating temperature or below. Normally, the HS_5 (monitor_1), the HS_1 (monitor_2) and HS_2 (monitor_3) are the hottest spot, so can assume these three hot spots surface temperature (cold plate side) as the case temperature.



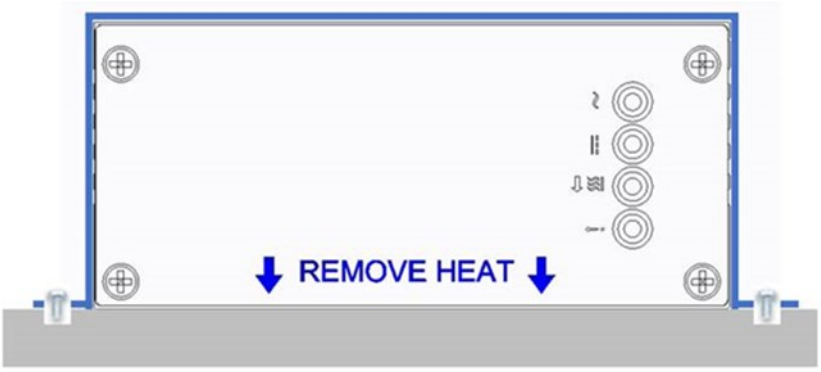
"Cooling side" (for heat transfer) is the large surface at the bottom of "Remove Heat" (opposite the label; closest to the Fault light; farthest from the blind-mate connector). The cooling device (cold plate, warm wall or heat sink) should be placed in good thermal contact with the entire cooling surface by using thermal grease or a thermal interface pad between them.

Application Notes:

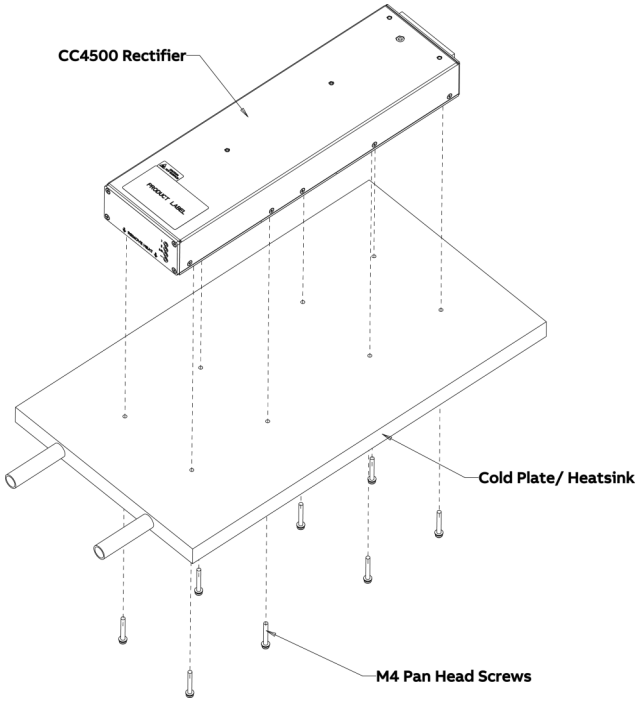
There are 2 options for installing the module with cold plate/Heatsink:

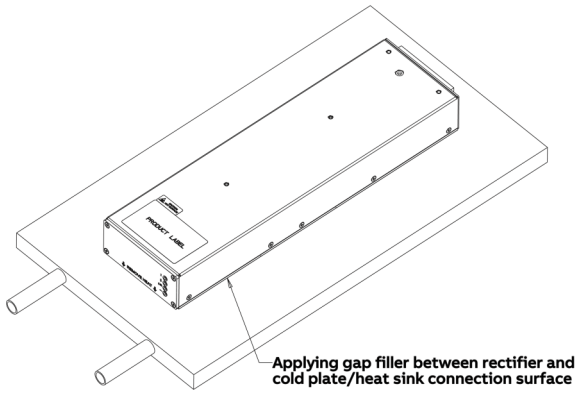
Option 1: To connect PSU externally to cold-plate, use external bars.

Apply gap filler, Laird T-putty 504, or other equivalent material, Thermal Conductivity is no less than 1.8 W/mK between the unit and cold plate/heatsink



Option 2: Install the module to the cold plate/heatsink with 8 M4x07 pan head screw from cold plate /heatsink bottom. Recommended Torque: 1.2Nm.3. Same way for CC4500 like with CC3500 below.





Accessories

Item	Description	Ordering code
	Single-unit cable assembly that mates with rectifier Blind-Mate connector (sold as a component, equipment containing this harness requires safety certification).	850045138
	1U_CP3500_interface: Rectifier interface board. This debug tool can be used to evaluate the performance of the rectifier at room temperature. The input interface is a standard IEC 320 C20 type socket. Outputs are connected via standard 0.25 fast-ons.	150039572
	Isolated Interface Adapter Kit – interface between a USB port and the I²C connector on the rectifier interface board. Includes a cable set to the PC and to the OmniOn HE-10 Connection.	150036482
	The site below downloads the OmniOn Digital Power Insight™ software tools, including the PRO_GUI_III.  When the download is complete, icons for the various utilities will appear on the desktop. Click on to start the program after the download is complete. **https://www.omnionpower.com/campaign/digitalpowerinsight**	Free download
	Graphical User Interface Manual: the GUI download created a directory. In that directory start the DPI_manual.pdf file.	

Ordering Information

Please contact your OmniOn Sales Representative for pricing, availability and optional features.

Item	Description	Ordering code
CC4500AC55FB	4.5kW Rectifier with blind-mate connector (short model); VO range 40-58V	1600483828A

Change History (excludes grammar & clarifications)

Revision	Date	Description of the change
1.0	02/21/2023	Initial release
1.1	01/03/2024	Updated as per OmniOn template
1.2	04/12/2024	Removed all references to Fast_Proc_Hot and updated part name and ordering code

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